

Programmes After Market Services NPL-1 Series Cellular Phones

2 – Baseband System

Table of Contents

Description	Page No.
Introduction	5
Abbreviations	5
Environmental specification	7
Absolute maximum ratings	7
Normal and extreme voltages	7
Temperature conditions	8
Humidity and water resistance	8
Vibration and bump	8
EMC / ESD immunity	8
Technical specifications	8
UEM	8
Reset sequence	8
No supply	10
Backup	11
Power off	11
Reset	11
Power on	11
Sleep	11
Protection mode	12
DC characteristics	12
Charging	16
Battery	17
UPP (Universal Phone Processor)	18
Bluetooth	22
UI	22
LCD cell	22
LCD Backlight	24
Keyboard light	25
LED driver circuit	25
Vibra	25
Buzzer	25
Keypad	26
IR-module	26
SIM	26
Memory description	27
Read cycle	28
Write cycle	28
Power saving signal (PS)	29
Memory block	31
Block locking	31
Read while write (RWW)	32
Burst mode	32

	Description	Page No.
Flash programming		33
MCU boot		34
Flash identifiers		34
First word		34
Second word		34
Third word		34
Fourth word		34
Fifth word		34
Absolute maximum ratings (AMD 64bit)		35
Absolute maximum ratings (INTEL 64bit)		35
HW Interfaces		36
Keypad interface		36
LCD interface		37
SIM interface		38
Ostrich		39
JTAG interface		39
BT module interface		40
SW interface		40
BT102 flash programming		40
HW interface		41
Baseband - RF interface		43
Digital signals		43
Analogue signals		45
Voltage supplies and references		46
MBus		49
FBus		49
SIM and keypad		49
Test Points		49

List of Figures

Figure 1	NPL-1 Baseband block diagram	6
Figure 2	UEM state diagram	9
Figure 3	LCD worst case test image	15
Figure 4	Baseband power distribution	16
Figure 5	Charging configuration	17
Figure 6	Detection of charger	17
Figure 7	UEM charging state diagram, PWM mode only	18
Figure 8	Charging scenario where the battery is abruptly removed	19
Figure 9	Mechanical layout of DCT-3 battery	20
Figure 10	UPP architecture	21
Figure 11	Complete overview of LCD module	23
Figure 12	LCD module	24
Figure 13	LED driver circuit for display	25

	Description	Page No.
List of Figures (continued)		
Figure 14	NPL-1 IR connectivity	26
Figure 15	UPP, UEM and SIM connections	27
Figure 16	Basic reading (random access)	28
Figure 17	Write waveform (random access)	29
Figure 18	The data is compared by using an XOR-function	30
Figure 19	The comparison shows more unequal bits	30
Figure 20	Burst mode reading from the flash	33
Figure 21	NPL-1 keypad	36
Figure 22	Placement of SIM pins (phone bottom view)	38
Figure 23	SW interface diagram	40
Figure 24	BT102 Flash programming	40
Figure 25	BT102 HW interface	41
Figure 26	XEAR connection	50
Figure 27	XMIC connection	51
List of Tables		
Table 1	Absolute max. ratings	7
Table 2	Temperature conditions for NPL-1	8
Table 3	UEM regulator outputs and state in SLEEP	12
Table 4	NPL-1 current consumption from VFLASH during SLEEP mode	13
Table 5	Regulator usage in NPL-1	14
Table 6	LCD current consumption	24
Table 7	Absolute max. ratings for AMD 64Mbit	35
Table 8	Absolute max. ratings for Intel 64Mbit	35
Table 9	LCD module pin-out to PWB	37
Table 10	SIM connector interface	38
Table 11	Ostrich interface	39
Table 12	JTAG interface levels	39
Table 13	BT - BB interface description	41
Table 14	Digital signals	44
Table 15	Analog signals	45
Table 16	Regulators and references	46
Table 17	MBus interface	49
Table 18	FBus interface	49

Introduction

This Chapter specifies the baseband module for the NPL-1 program. The baseband module includes the baseband engine chipset, the UI components and the acoustical parts for the transceiver.

NPL-1 is a hand-portable GSM900/GSM1800 phone for the classic segment, having the DCT4 generation baseband- and RF circuitry. The key drivers for this product are time to market, FFR and RF performance.

The mechanical solution is based on the NPE-3 phone, modified with a new A-cover design. The acoustical design is very similar to that implemented in NPE-3.

NPL-1 is having the DCT3 system connector and supports accordingly most DCT3 accessories. The battery interface is the one known from DCT3 phones and NPL-1 will support both Nickel- and Lithium batteries.

New features in NPL-1 project are Bluetooth wireless data and audio connection, GPRS for TCP/IP protocol data transmission, as well as triple band RF.

Abbreviations

BSI	Battery Size Indicator
NO_SUPPLY	UEM state where UEM has no supply what so ever
VBAT	Main battery voltage
V_{MSTR+}, V_{MSTR-}	Master Reset threshold level (2.1 V / 1.9 V)
VBACK	Backup battery voltage
V_{BU_{COFF+}}, V_{BU_{COFF-}}	Backup battery threshold level (3.1 V / 2.8 V)
BACK_UP	UEM state where UEM has backup voltage
RESET	UEM state where regulators are enabled
RTC	UEM internal Real Time Clock
VRTC	Regulator voltage for RTC
PWR_OFF	UEM state where phone is off
SLEEP	UEM power saving state controlled by UPP
SLEEPX	SLEEP control signal from UPP
PWRONX	Signal from power on key. '1' = key pressed.
VCHAR	Charger input voltage
VCHAR_{DET}	Charger detection threshold level
UEM	Universal Energy Management
UPP	Universal Phone Processor
IMD	In-Mould Decoration

Technical Summary

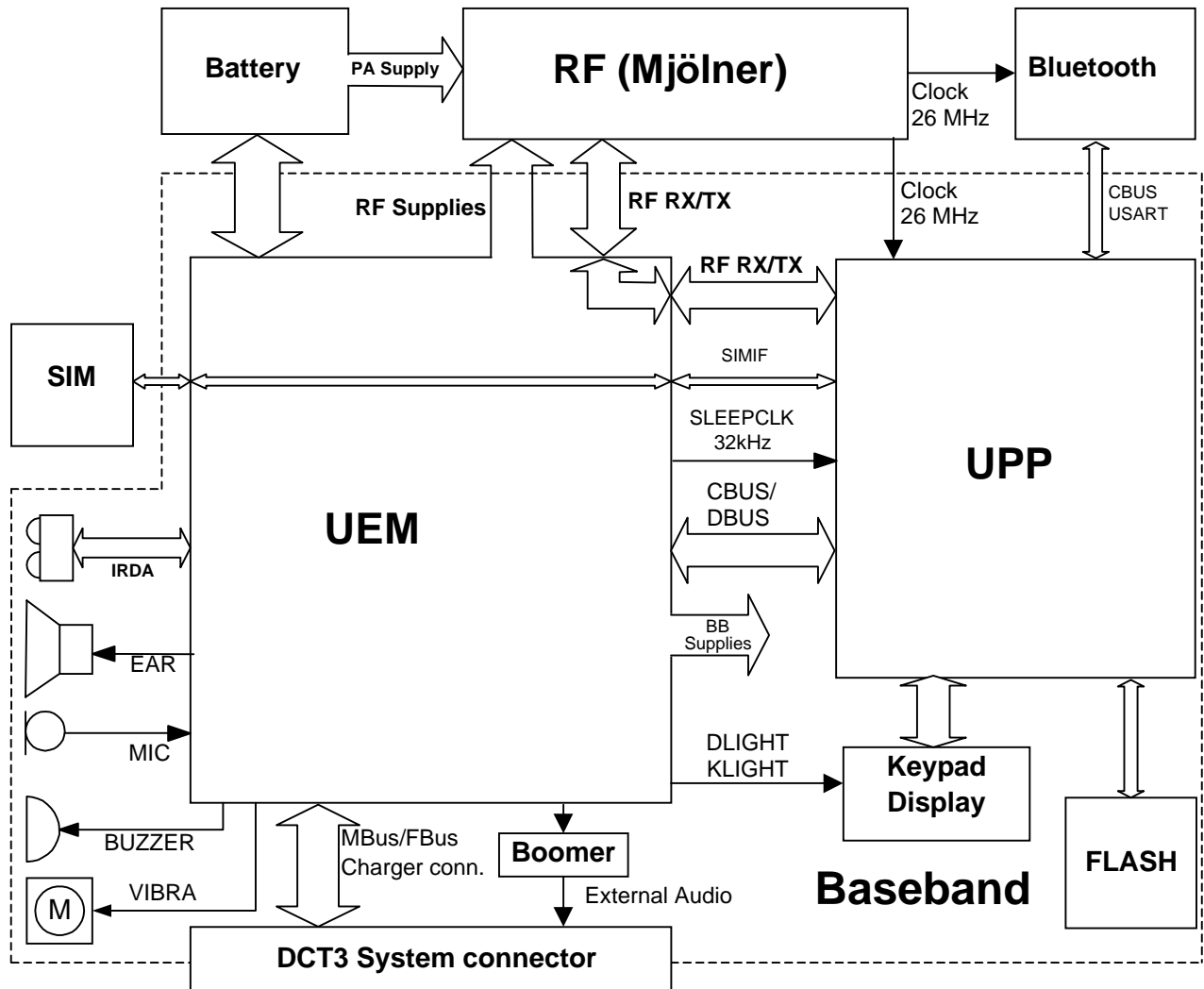


Figure 1 NPL-1 baseband block diagram

A draft block diagram is shown in Figure 1 NPL-1 baseband block diagram.

The baseband module contains 2 ASICs namely the **Universal Energy Management (UEM)** and the **Universal Phone Processor (UPP)**. The baseband module furthermore contains the Bluetooth module. The baseband is based on the DCT4 engine program.

The UEM supplies both the baseband module as well as the RF module with a series of voltage regulators. Both the RF module and baseband module are supplied with regulated voltages 2.78 V and 1.80 V. The UEM is furthermore supplying the baseband SIM interface with a programmable voltage of either 1.8 V or 3.0 V and the core of the UPP is supplied with a programmable voltage of 1.0 V, 1.3 V, 1.5 V or 1.8 V.

The UEM contains a series of PWM sourced drivers. The individual PWM signals are generated internally within the digital part of the UEM and distributed to the drivers. The buzzer driver receives a PWM signal where both frequency and duty-cycle are pre-set by

register writings. For the vibra, a set of frequencies can be chosen. The frequencies are 64 Hz, 128 Hz, 258 Hz and 520 Hz and the duty cycle 2.9 % to 96.9 %. LCD and keyboard light LED drivers receive a PWM signal of 128 Hz where the duty-cycle can be programmed by setting a 4-bit register.

The UEM also contains an IR driver supporting 9600 bps to 1152 kbps, semi duplex. This driver works as a level shifter on the RX and TX lines to and from the UPP.

The UEM contains a real-time clock sliced down from the 32768 Hz crystal oscillator. The 32768 Hz clock is fed to the UPP as a sleep clock.

The communication between the UEM and the UPP is done on the bi-directional CBUS and DBus. The CBUS is controlled by the MCU and can operate at a speed of maximum 1 MHz. The DBus is controlled by the DSP and can operate at a maximum speed of 13 MHz. Both processors are located in the UPP.

Environmental Specifications

Absolute maximum ratings

Table 1: Absolute maximum ratings

Parameter	Rating	Remarks
Supply voltage, VBAT	-0.3 V to 5.5 VDC	Supply voltage for UEM
Charger input voltage, VCH	-0.3 V to 16 VDC -0.3 to 20 VDC _{pk}	Conditions set by UEM. Input clamped @16 VDC.

Normal and extreme voltages

Nominal voltage:	3.6 V	(VBAT, Main battery voltage)
Lower extreme voltage:	2.9 V	(V _{COFF-} , Hardware cut-off voltage)
Higher extreme voltage	5.4 V	(VBAT _{LIM2+} , Upper charger limit)
Conditions set by UEM.		
Minimum guaranteed operating voltage	3.04 V	(DCT4 Engine minimum cut-off voltage)

Temperature Conditions

Table 2: Temperature conditions for NPL-1

Environmental condition	Ambient temperature	Remarks
Normal operation	-25 ° C ... +55 ° C	Specifications fulfilled
Reduced performance	+55 ° C ... +70 ° C	Operational for short periods only
No operation or storage	-40 ° C > T > 85 ° C	No storage. An attempt to operate may damage the phone permanently
Long term storage conditions	0 ° C ... +40 ° C	Condition is without battery

Humidity and water resistance

The baseband module will comply with the SPR4 Operating Conditions.

Vibration and bump

The baseband module will comply with the SPR3 Mechanical Functionality.

EMC / ESD immunity

The baseband module will comply with the SPR4 Operating Conditions. See also baseband EMC strategy in section SIM and keypad on page SIM and keypad.

Technical Specifications

The following chapters describe the NPL-1 baseband module in overview. If further information is needed, check with the references at the end of the Specification section References and/or with references mentioned in the individual chapters.

UEM

The UEM is one of the two ASICs in the baseband module.

Reset sequence

The functional behaviour of the UEM can be divided into 7 different states. Since the UEM controls the regulated power distribution of the phone, each of these states affects the general functionality of the phone:

- No supply
- Backup
- Power off
- Reset
- Power on
- Sleep
- Protection

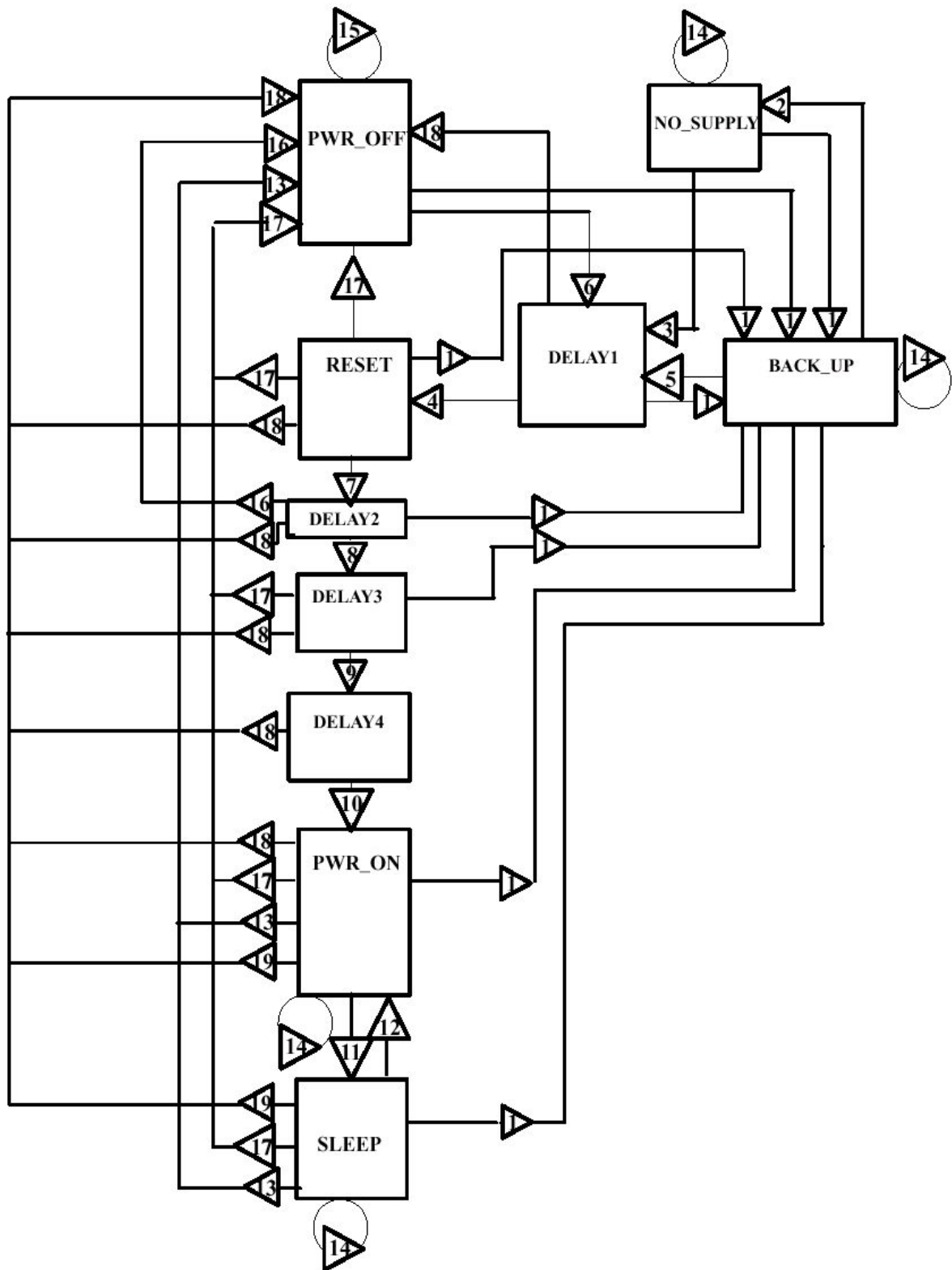


Figure 2 UEM state diagram

The text below explains the state diagram. The symbol ' \nearrow ' means that the voltage rises and ' \searrow ' that the voltage drops. ' \rightarrow ' Means the result of the conditions set on the left most side.

$V_{BAT} < V_{MSTR}$ and $V_{BACK} > V_{BU_{COFF}}$ \rightarrow Go to BACK_UP

$V_{BAT} < V_{MSTR}$ and $V_{BACK} < V_{BU_{COFF}}$ \rightarrow Go to NO_SUPPLY

$V_{BAT} \nearrow V_{MSTR+}$. $V_{BACK} < V_{BU_{COFF}}$ \rightarrow Go to DELAY1

$V_{BAT} > V_{MSTR}$. DELAY1 elapses \rightarrow Go to RESET

$V_{BAT} \nearrow V_{MSTR+}$. $V_{BACK} > V_{BU_{COFF}}$ \rightarrow Go to DELAY1

$PWRONX = '0'$ or $VCHAR \nearrow VCHAR_{DET+}$ or $ALARM = '1'$ \rightarrow Go to DELAY1

$V_{BAT} > V_{COFF+}$ \rightarrow Go to DELAY2

DELAY2 elapses \rightarrow Go to DELAY3

$V_{BAT} > V_{COFF+}$. DELAY3 elapses \rightarrow Go to DELAY4

DELAY4 elapses \rightarrow Go to PWR_ON

$SLEEPX = '0'$ \rightarrow Go to SLEEP

$SLEEPX = '1'$ \rightarrow Go to PWR_ON

$V_{BAT} \searrow V_{COFF-}$ and $V_{BAT} > V_{MSTR-}$ \rightarrow Go to PWR_OFF

No change

$V_{BAT} > V_{MSTR}$ \rightarrow Stay in PWR_OFF

$PWRONX \nearrow$ detection during DELAY2 \rightarrow Go to PWR_OFF

Watchdog elapses (approx. 100 μ s) \rightarrow Go to PWR_OFF

Thermal shutdown \rightarrow Go to PWR_OFF

PwrKeyWatchdog (4 sec.) elapses \rightarrow Go to PWR_OFF

The different states of the UEM are explained further below:

No supply

In the NO_SUPPLY mode the UEM has no supply voltage ($V_{BAT} < V_{MSTR}$ and $V_{BACK} < V_{BU_{COFF}}$). This mode is due to the fact, that both the main battery and the backup battery is either disconnected or both discharged to a low voltage level.

The UEM will recover from NO_SUPPLY into RESET mode if the VBAT voltage level rises above the V_{MSTR+} level by either reconnecting the main battery or charge it to such level.

Backup

In BACK_UP mode the main battery is either disconnected or has a low voltage level ($V_{BAT} < V_{MSTR-}$ and $V_{BACK} > V_{BU_{COFF+}}$).

The regulator VRTC that supplies the real time clock is disabled in BACK_UP mode. Instead the unregulated backup battery voltage VBACK supplies the output of the VRTC. All other regulators are disabled and the phone has no functionality.

The UEM will recover from BACK_UP mode into RESET mode if VBAT rises above V_{MSTR+} .

Power off

In order for the UEM to be in PWR_OFF mode, it must have supply voltage ($V_{BAT} > V_{MSTR+}$).

The regulator VRTC regulator is enabled and supplying the RTC within the UEM. The UEM will enter RESET mode after a 20 ms delay whenever one of the below listed conditions is logically true:

- The power button is activated
- Charger connection is detected
- RTC alarm is detected

The UEM will enter PWR_OFF from all other modes except NO_SUPPLY and BACK_UP if the internal watchdog elapses.

Reset

When the UEM enters RESET mode from PWR_OFF mode the watchdog is enabled. If the VBAT fails to rise above the power-up voltage level V_{COFF+} (3.1 V) before the watchdog elapses, the UEM will enter PWR_OFF mode. Otherwise after a 200 ms delay the regulator VFLASH1 will be enabled and after a additional delay of 500 μ s the regulators VANA, VIO, VCORE and VR3 will be enabled. All other regulators i.e. VFLASH2, VSIM, VR1, VR2 and VR4 – VR7 are software controlled and disabled by default. After an additional delay of 20 ms the UEM enters PWR_ON mode.

Power on

In PWR_ON the UEM is fully functional in the sense that all internal circuits is powered up or can be by means of software. The UEM will enter PWR_OFF mode if VBAT drops below V_{COFF-} for a period of time longer than 5 μ s. The UEM will furthermore enter PWR_OFF mode if either of the watchdogs Operational State Machine (approx. 100 μ s), Security (32 sec.) or Power Key (4 sec.) elapses or if any of the regulators triggers the thermal protection circuitry

Sleep

The UEM can be forced into SLEEP mode by the UPP by setting the input SLEEPX low for more than 60 μ s. This state is entered when the external UPP activity is low (phone in

sleep) and thereby lowering the internal current consumption of the UEM. The regulator VANA is disabled and VR1 – VR7 are either disabled or in low quiescent mode.

From SLEEP the UEM enters PWR_ON if SLEEPX goes high, PWR_OFF mode if watchdog elapses or BACK_UP mode if VBAT drops below V_{MSTR-} .

Protection mode

The UEM has two separate protection limits for over temperature conditions, one for the charging switch and one for the regulators. The temperature circuitry measures the on-chip temperature. In case of charging over temperature, the circuit turns the charging switch off. In case of over temperature in any of the regulators, the UEM powers off.

DC characteristics

The figures in the following table reflect the specifications of the voltage and current regulators within the UEM.

Table 3: UEM regulator outputs and state in sleep

Regulator	Target	Output Voltage [V]			Output Current [mA]		UEMSLX = '0' ⁴
		Min	Typ	Max	Min	Max	
VR1A, VR1B	RF	4.6	4.75	4.9	0	10	Off
VR2 ⁶	RF	2.70	2.78	2.86	0.1	100	Off or Low Iq
VR3	RF	2.70	2.78	2.86	0.1	20	Off
VR4 ²	RF	2.70	2.78	2.86	0.1	50 0.1	Off
VR5, VR6 ²	RF	2.70	2.78	2.86	0.1	50 0.1	Off
VR7	RF	2.70	2.78	2.86	0.1	45	Off
VrefRF01	RF	1.334	1.35	1.366	-	0.1	On
VIO ²	BB	1.72	1.8	1.88	0.1 0.005	150 0.500	Low Iq
VSIM ²	BB	1.745 2.91	1.8 3.0	1.855 3.09	0.005 0.005	25 0.500	Low Iq
VANA	BB	2.70	2.78	2.86	0.005	80	Off
VCORE ³	BB	1.000 1.235 1.425 1.710 0.974 1.215 1.410 1.692	1.053 1.3 1.5 1.8 1.053 1.3 1.5 1.8	1.106 1.365 1.575 1.890 1.132 1.365 1.575 1.890	0.005 0.005 0.005 0.005 70 85 100 120	70 85 100 120 200 200 200 200	Low Iq
VFLASH1	BB	2.70	2.78	2.86	0.005 0.005	70 1.5	Low Iq
VFLASH2 ⁵	BB	2.70	2.78	2.86	0.005	40	On or Off

- 1) Controlled by MCU writing to UEM references register.

- 2) The second current value indicates the maximum possible output current of the regulator when in low quiescent mode.
- 3) The output voltages are split into two different current categories. The upper part is the lower range of output current, and the lower part is the higher range of output current.
- 4) UEMSLX is slave to SleepX from the UPP. Sets the UEM into sleep mode.
- 5) Condition in sleep-mode depends on MCU writings to UEM regulator registers solely.
- 6) Condition in sleep-mode depends on DSP writings to UEM register.

Table 4: Regulator usage in NPL-1

Voltage	Typ. Value	Max. output current	On/Off controlled by	Low quiescent mode controlled by	Main loads	Typ, current consumption	Max. current consumption
VBAT	3.6V	n.a.	n.a.	n.a.	UEM: VBATBB1 ...5, VBATVR1 ...7, VBATDRIV		
					Audio	0.1µA / 5mA /	2µA / 10mA / 30mA _{AV}
					LPRF: VCC	80µA / 0.5mA / 35mA	160µA / 0.6mA / 37mA
					IrDa: LEDA		400mA _p
					LEDs	31mA	
					Buzzer		200mA
					Vibra		200mA
					RFPA		1.85A _p
VANA	2.78V	80mA	SLEEPX	n.a.	UEM: VDAAUD2		
					UEM: VDACONVRX		
					UEM: VDACONVTX		
					MicBias (int. +ext.)		
					Pull Ups		
VFLASH1	2.78V	1.5mA/70mA	UEM Logic	SLEEPX	UEM: VDD28		
					LCD: VDD		
					LPRF: VREG		
					IrDa: VCC		
					Pull Ups		
VFLASH2	2.78V	40mA	MCU	n.a.	DCT3-ACCs (DLR-3P)		
VIO	1.8V	0.5mA/150mA	UEM Logic	SLEEPX	UEM: VDD18		
					UPP		
					Flash		
					LCD: VDDI		
					LPRF: VAPPL		
					Mjoelner: VDDDL		
VCORE	1.0V / 1.3V / 1.5V / 1.8V	0.2mA/200mA	UEM Logic, MCU	SLEEPX	UPP		
VSIM	1.8V / 3.0V	0.5mA / 25mA	MCU	SLEEPX	SIM card		

Table 4: Regulator usage in NPL-1

Voltage	Typ. Value	Max. output current	On/Off controlled by	Low quiescent mode controlled by	Main loads	Typ. current consumption	Max. current consumption
VR1A	4.75V	10mA	DSP	n.a.	Mjoelner: VDDCP	0 / 0.45mA	
VR1B	4.75V	10mA	DSP	n.a.			
VR2	2.78V	0.1mA / 100mA	DSP	DSP	Mjoelner: VDDDIG	0 / 50µA / 10mA	
					Mjoelner: VDDTX	0 / 8.5mA	
					TX-Modulators	0 / 66mA	
VR3	2.78V	20mA	SLEEPX	n.a.	Mjoelner: VDDBBB	0 / 0.6mA	
					Mjoelner: VDDX0 (26MHz)	0 / 1.1mA	
					RFCLK-Buffer	1mA	
VR4	2.78V	0.1mA / 50mA	DSP & SLEEPX	DSP	Mjoelner: VDDRBBB (+VTXB_900 (Buffer))	0 / 37mA / 14mA	
VR5	2.78V	0.1mA / 50mA	DSP & SLEEPX	DSP	Mjoelner: VDDL0	0 / 18mA / 26mA	
					Mjoelner: VDDPRE	0 / 6.5mA	
					Mjoelner: VDDPLL	0 / 1mA	
VR6	2.78V	0.1mA / 50mA	DSP & SLEEPX	DSP	Mjoelner: VDDRXF	0 / 9mA	
VR7	2.78V	0.1mA / 50mA	DSP & SLEEPX	DSP	VCO (3.xGHz)	18mA	

Due to the low output current from the VFLASH1 regulator during sleep, the following table with estimated current consumption drawn from the regulator in sleep mode was made.

Table 5: NPL-1 current consumption from VFLASH1 during Sleep mode

Consumer	Max current	Unit	Note
LCD ¹	376	µA	All figures are estimates @25 °C
Audio area - XMIC	60		
- XEAR	1		
- DLR-3P	1		
Bluetooth	8		
UEM - 2 x slow ADC	2		
- BSI	29		
IR	5		
Total	482		

1) Maximum current measured on 10 samples.

The current consumed by the LCD has been measured by vendor using worst case normal

mode displayed image as shown in Figure 3.

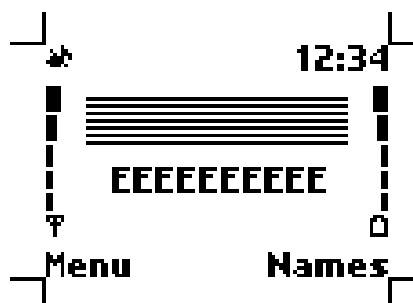


Figure 3 LCD worst case test image

Under normal conditions, the battery powers the baseband module. The battery voltage VBAT is regulated by individual regulators located within the UEM. These regulators supply the different parts of the phone. 8 regulators are dedicated to the RF module of the phone, and 6 to the baseband module.

The VSIM regulator is able to deliver both 1.8 and 3.0 Vdc and thus supporting two different SIM technologies. A register internally in the UEM controls the output of VSIM and can be written to by the MCU via the CBUS. The regulator VCORE is likewise adjustable and controlled by register writings by the MCU. VCORE supplies the core of the UPP and can be adjusted on the fly by the MCU if DSP capacity is inadequate. Higher VCORE supply (1.8 V) results in faster core operations in the UPP.

The regulator VFLASH2 supplies audio circuitry and is controlled by the MCU

The regulators VANA, VFLASH1 and VIO are solely controlled by the UEM and cannot be en-/disabled by MCU writings. Furthermore, VFLASH1 and VIO are both ON, though in low quiescent mode when the phone is in sleep mode. An output current of 500 µA can be drawn from the VIO regulator and 1.5 mA from the VFLASH1 regulator. VIO supplies the UPP, FLASH and LCD, VFLASH1 supplies LCD, DLR-3 cable, IRDA and the Bluetooth module. VANA is supplying analogue parts internally in the UEM as well as the baseband audio circuitry and pull-up resistors on the input of the UEM slow AD converters.

When the plug and play DLR-3 cable is connected to the phone, it must be supplied by the phone with 2.78 Vdc / 25 mA. This is delivered via a switch from VFLASH1. The switch is controlled by the MCU and the control signal originates from a general IO pin on the UPP.

The regulators VR1A, VR1B, VR2 – VR7 and IPA1 – IPA4 are all controlled by the DSP via the DBus. VR3 – VR7 are controlled by the UEM as well and are disabled in sleep regardless of DSP writings.

VBAT is furthermore distributed, unregulated, to the RF power-amplifier and the BT102 Bluetooth module as well as filters in the baseband module.

The CHACON module in the UEM controls the charging of the main battery. Furthermore it contains a 3.2 Vdc regulator for charging of the backup battery and a 1.8 Vdc regulator supplying the internal real time clock.

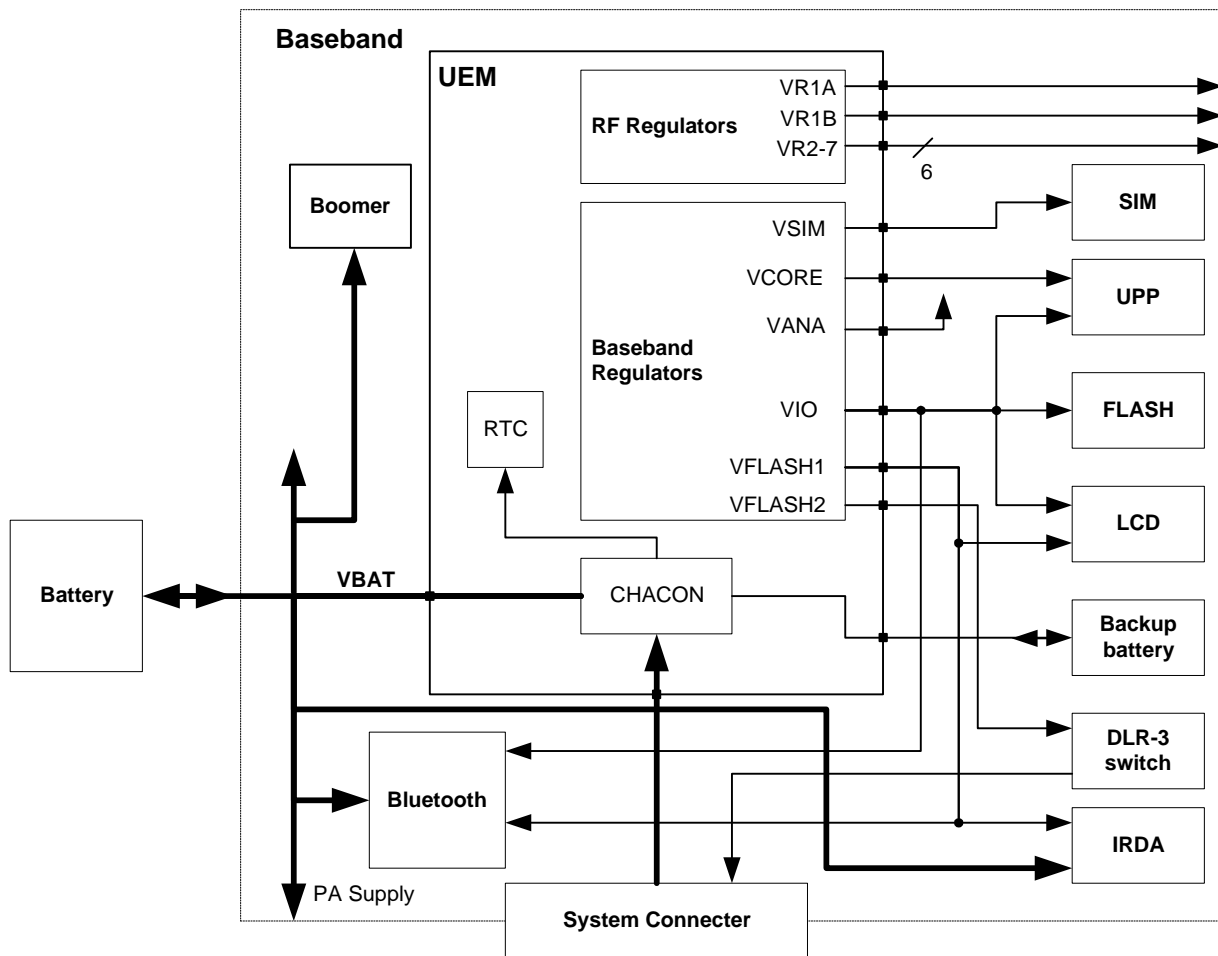


Figure 4 Baseband power distribution

Charging

The charging of the main battery is controlled by the UEM. External components are needed in order to sense charging current and voltage that are needed by the Energy Management (EM) software and to protect against EMC into the baseband area. The charger is connected to the phone via the DCT3 bottom connector and routed from here

to the UEM via the PWB.

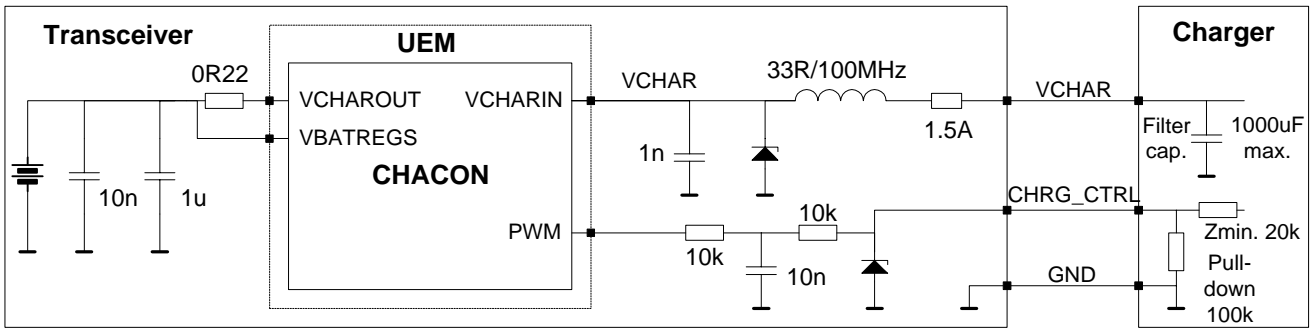


Figure 5 Charging configuration

Connecting a charger to the telephone creates a voltage, VCH, on the UEM VCHAR input. When the VCH level is detected to rise above the VCH_{DET} threshold ($2.0 V_{dc}$) by CHACON, charging starts. Level crossing detection of the VCHAR line is used to generate synchronizing pulses for UEM's state machine for control of rectifier type chargers, e.g. ACP-7.

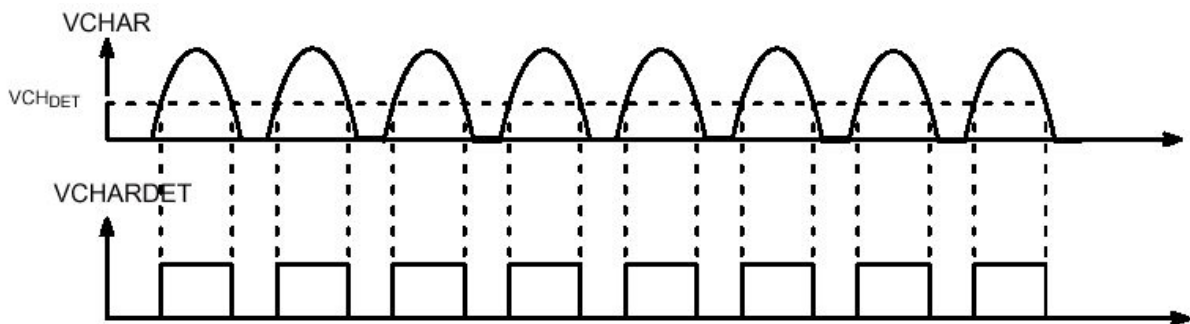


Figure 6 Detection of charger / generation of charger synchronization pulses

In case the main battery is fully discharged and the UEM subsequently is without power i.e. in NO_SUPPLY or BACKUP mode, the start-up charging circuitry is in control, giving the possibility to detect a charger and engage charging. If the VBAT level is detected to be lower than the master reset voltage (V_{MSTR-}) the CHACON will charge the battery with a constant current of 100 mA until VBAT exceeds V_{MSTR+} . When this happens, from a charging point of view, normal PWM charging situation resumes. A PWM signal is generated by the digital part of the UEM, which sources the CHACON. The frequency of the signal can be either 1 Hz or 32 Hz. If the connected charger is of a 2-wire kind e.g. ACP-7, the PWM signal has the frequency 1 Hz. If the charger on the other hand is a 3-wire type e.g. ACP-9, the switch is left on permanently and the 32 Hz PWM control signal routed to the charger in order to produce a constant voltage. Figure 7 shows a state diagram of the PWM charge situation.

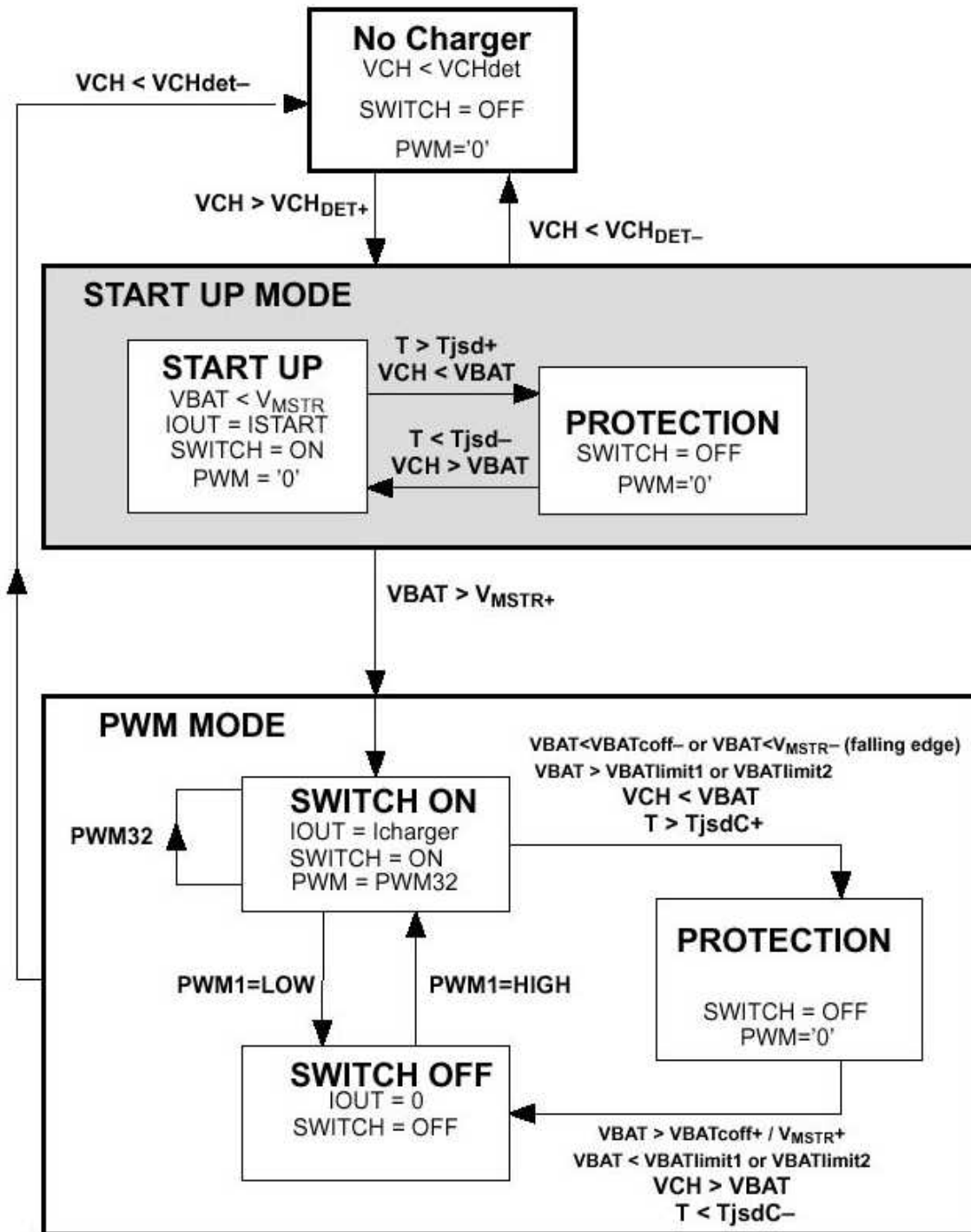


Figure 7 UEM charging state diagram, PWM mode only

In order to protect the phone from damage resulted by over voltage in the case that the battery is abruptly removed when charging is ongoing, the charger switch is closed immediately. This is detected by means of VBAT that will rise fast above $V_{BAT_{LIM1,2+}}$ when the battery is removed. A scenario like this can be seen in Figure 8.

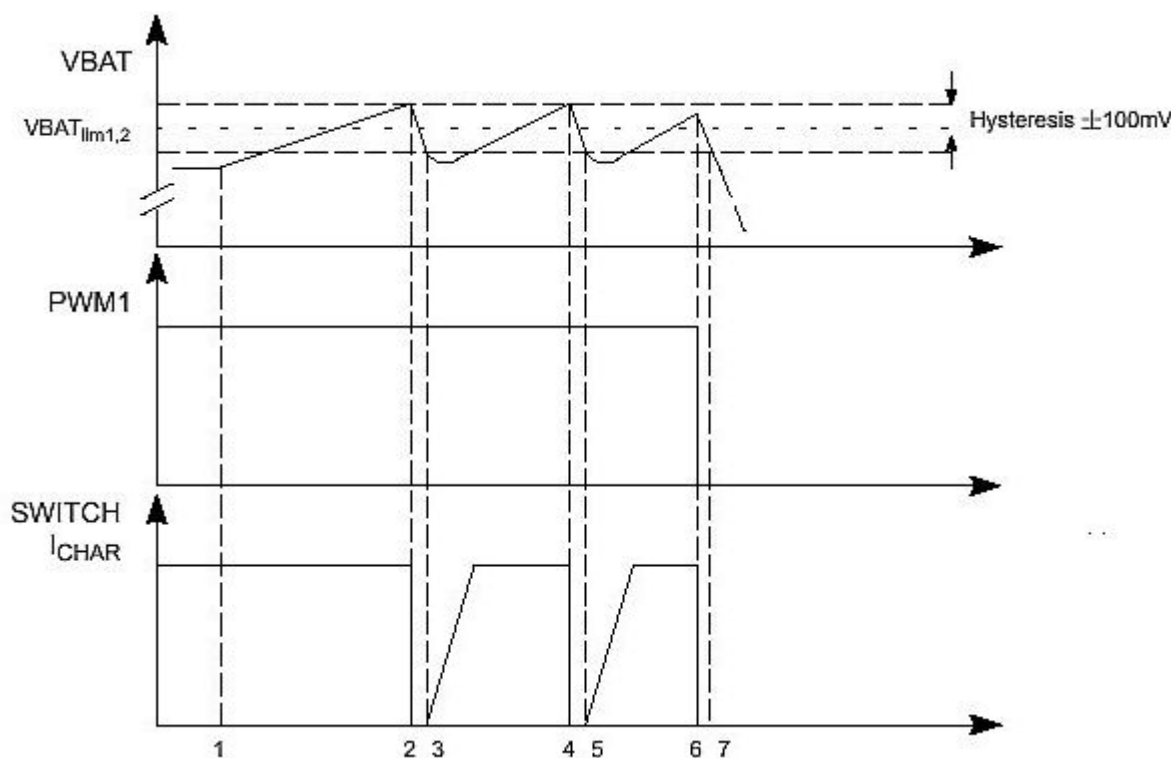


Figure 8 Charging scenario where the battery is abruptly removed

- 1) Battery disconnected abruptly during charging
- 2) VBAT reaches $V_{BAT_{LIM1,2+}}$ → charging switch is turned off immediately
- 3) VBAT falls below $V_{BAT_{LIM1,2-}}$ → charging switch is turned on (soft switching)
- 4) VBAT reaches $V_{BAT_{LIM1,2+}}$ again → charging switch is turned off
- 5) VBAT falls below $V_{BAT_{LIM1,2-}}$ once again → charging switch is turned back on
- 6) The PWM signal from the UEM digital part turns logical '0' because the system has acknowledged the absence of a battery and this subsequently turns the charging switch off.
- 7) VBAT falls below $V_{BAT_{LIM1,2-}}$ but the charging switch is not turned back on since the PWM signal is logical '0'.

Note: that if the battery voltage level is below V_{MSTR-} level when the battery is disconnected from the phone, and if the charger is still connected when the battery is once again attached to the phone, the UEM will remain in NO_SUPPLY or BACKUP mode. This will keep the phone OFF until the charger is first disconnected and then reconnected.

Battery

The battery is external and will be connected to the phone via four terminals as shown in Figure 9. In order to detect the capacity and chemistry of the battery, the phone uses the

BSI connection in conjunction with 100 k Ω pull-up resistors in the baseband module or in the desk-stand DCH-9 extra battery slot, which allows charging of extra battery. 2.78 V from VFLASH1 feeds the resistor in the baseband module and the resulting divided voltage is routed to the BSI ADC input in the UEM.

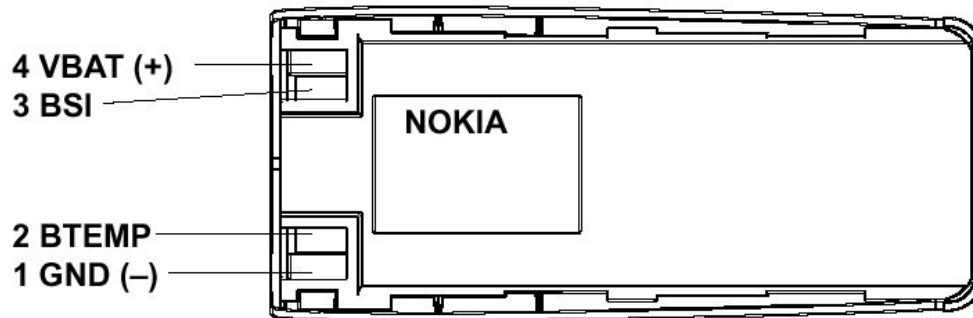


Figure 9 Mechanical layout of DCT-3 battery

The battery also contains a 47 k Ω NTC resistor used for battery temperature measurements. The measurement of the temperature by means of resistors follows the same principal as with the BSI resistor.

UPP (Universal Phone Processor).

The UPP used for NPL-1 is a version with 8 Mbit internally RAM. It is clocked by a 26MHz frequency from the RF-chip "Mjoelner".

It can operate on 4 different voltages; 1.05, 1.3, 1.5 and 1.8V. The voltage can be programmed "on the fly" by the SW. For example in standby-mode, 1.3V is used for power saving, but in active-mode (i.e. call) the voltages is increased to 1.8V to get maximum numbers of MIPS.

The UPP can be divided into two functional sections, Body and Brain. Body contains system logic, and Brain contains processor subsystem including DSP, MCU, memories and Bus Controller. The function of the Body is mainly the same as in DCT3 system Logic. The Body is connected to Brain via RHEA bus. The Body and Brain is shown below.

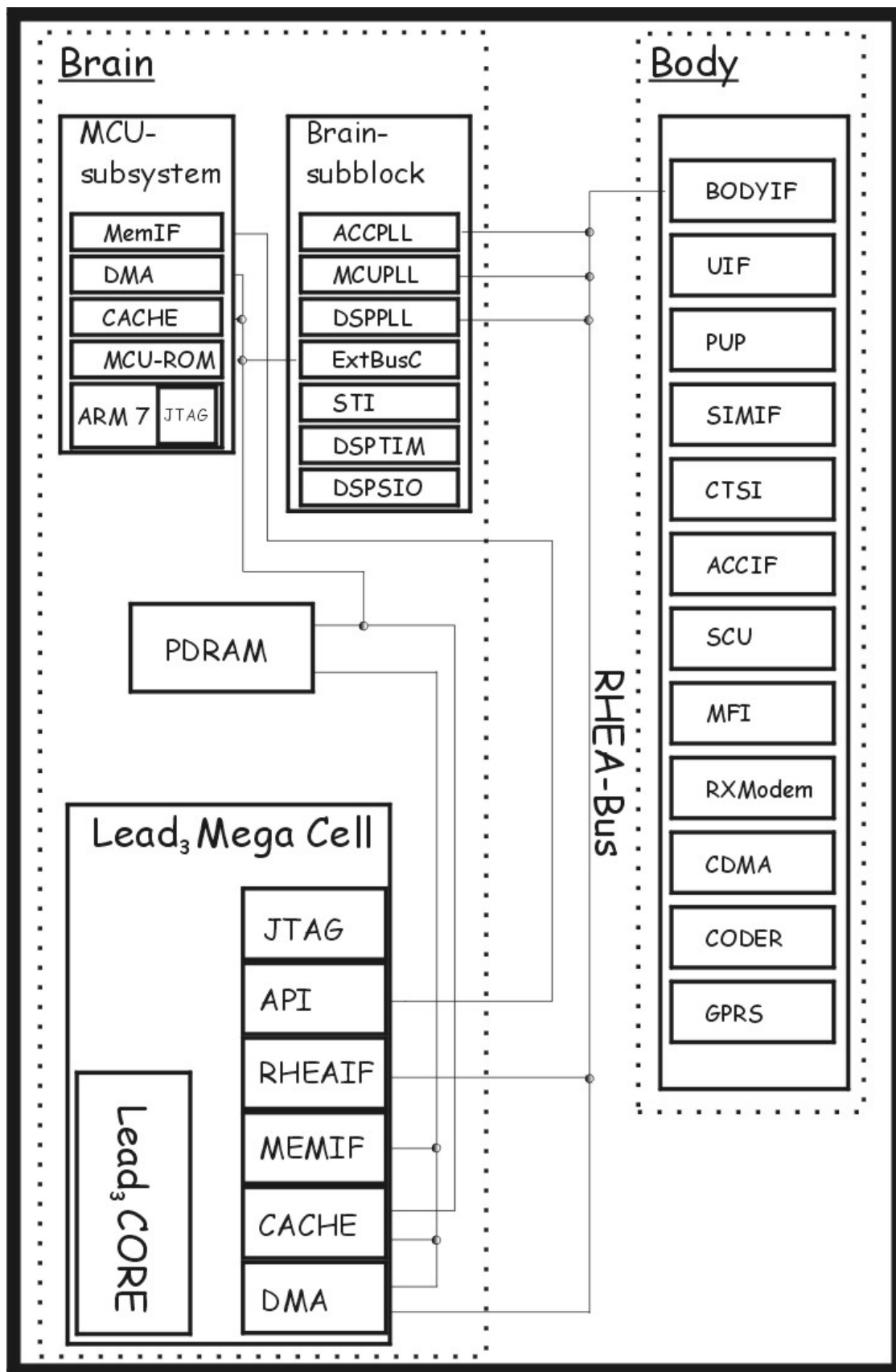


Figure 10 UPP architecture

The DSP inside the Brain is a Lead₃ 16-bit DSP core from TI (Texas Interments), with a DMA controller, wait state generator and a program fetch of 32-bits. Furthermore, the DSP core has an instruction-length flexibility of 8 to 48-bits. The maximum frequency for the DSP core is 145MHz for the NPL-1 baseband, although the maximum frequency for the core itself is 400 MHz. The core can do single and dual mac-operations per clock-cycle. This means that the NPL-1 baseband has a maximum of 290 MIPS (mac-operations) on the DSP-core.

The DSP core has three different RAM-banks; cache RAM, dual access RAM for storing and manipulating data and last, single access RAM for storing and manipulating SW variables. All the RAM-banks have a 145 MHz clock and 32-bit organization. It has also an ARM port interface, which is used for MCU/DSP message transfer (API).

The MCU consist of a 16/32-bit RISC core (ARM7). The block has a small ROM (768x32 bits) for MCU boot code. It interfaces to DSP through the 8Mbit PDRAM. The MCU has it own sectors in the RAM as well as the DSP. RAM blocks or sectors are divided into the following:

- 4 x 64Kbytes for the DSP and MCU.
- 4 x 64KB Banks, MCU only.
- 2 x 4KB Banks, for the DSP, and MCU.

The rest of the PDRAM is used for program code, mainly GPRS SW.

Bluetooth

NPL-1 has a Bluetooth module BT102 that receives and transmit at 2.4GHz. The module makes it possible for the phone to communicate via a radio link with other Bluetooth units e.g. headsets, carkits or printers.

The Bluetooth module is itself made as a multilayer PWB – covering all the needed Asics and discrete components – with a shielding frame- and lid. The module is soldered onto the phone PWB in the same way as other SMD components.

UI

LCD cell

The LCD is a black and white LS2 96x65 full dot matrix display. The LS2 display has a standard DCT4 interface. The LCD cell consists of a single COG driver, 3 boosting capacitors and a FPC, where the capacitors are placed. The LCD interface between the LCD cell and the main PWB can be viewed in section LCD Interface page LCD Interface.

The LCD cell is part of the complete LCD module, which includes metal frame, gasket, light guide, spring connector, RTC battery, translector (not shown) and dome sheet. The figure below illustrates the complete overview of the LCD module.

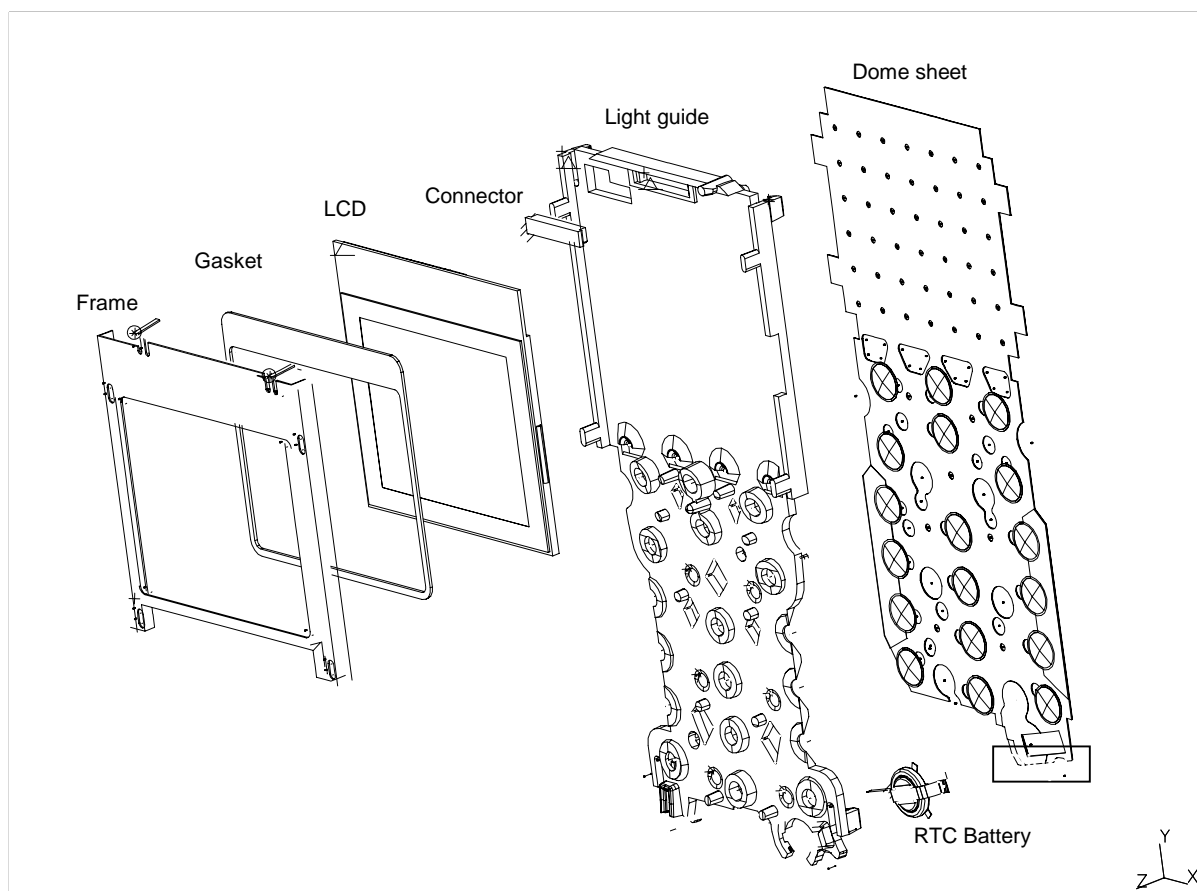


Figure 11 Complete overview of LCD module

Below is the general specifications listed:

- Glass size, width x height x thickness (incl. caps) : 38.4 mm x 37.6 mm x 2.75 mm
- Viewing area (width x height) : 35.4 mm x 27.7 mm
- Active pixel area (width x height) : 30.609 mm x 24.1 mm
- Number of pixels : 96 columns x 65 rows
- Pixel height to width ratio : 1.17:1
- Pixel gap : 0.015 mm
- Technology : FSTN
- Display type : Positive
- Main viewing direction : 6 o'clock
- Illumination Mode : Transflective
- Driver chip : DCT4 driver

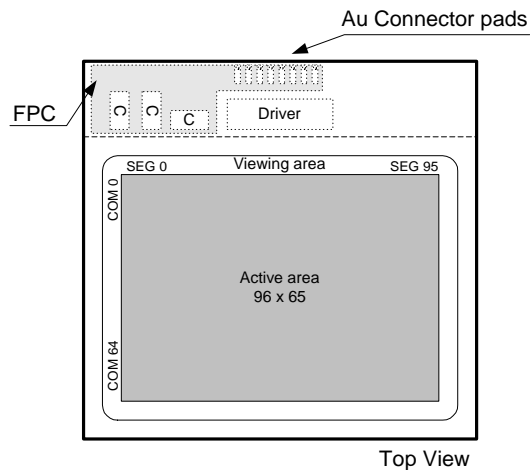


Figure 12 LCD module.

The LCD is powered from both V_{FLASH1} and V_{IO} . V_{FLASH1} is used for the boosting circuit and V_{IO} for the driver chip. The total LCD current consumption specified by vendor is described below:

Table 6: LCD current consumption

	Typ	Max	Unit/Note
I_{total}	250	400	$\mu A @ +25^{\circ}C$ $I_{total} = I_{DD} + I_{DDI}$ I_{total} is measured with normal mode test pattern.
		400	$\mu A @ T_{op}$, measured with normal mode test pattern.
	900	1300	μA using worst case test pattern @ $25^{\circ}C^1$

¹ This test pattern is used for R&D purpose only and is not possible to recreate by end user.

LCD Backlight

The LCD backlight consists of 4 white LED's (through hole type) which are placed on the main PWB below the LCD area. They shine into the light guide where the light is distributed to generate sufficient backlight for the LCD.

The LED driver circuit is shown below in Figure 13 LED driver circuit for display and key light. The voltage drop over R307 produces a constant current of 24 mA, i.e. 6 mA per LED.

The UEM output pin, DLIGHT, controls the driver circuit. This output is an open drain driver. The output frequency is 128 Hz and the duty cycle can be changed from 0 – 100 % with 4 bit resolution. By changing the duty cycle of the PWM signal it is possible to change the average current of the LED's.

Keyboard light

The keyboard light consists of 6 white LED's which are placed under the keyboard and use the light guide to distribute the light. The driver circuit is the same as described above in section LCD Backlight, with the difference of a current of about 9 mA, i.e. 1.5 mA per. LED.

The keyboard LED's can also be controlled by a 128 Hz PWM signal from the UEM, KLIGHT.

LED driver circuit

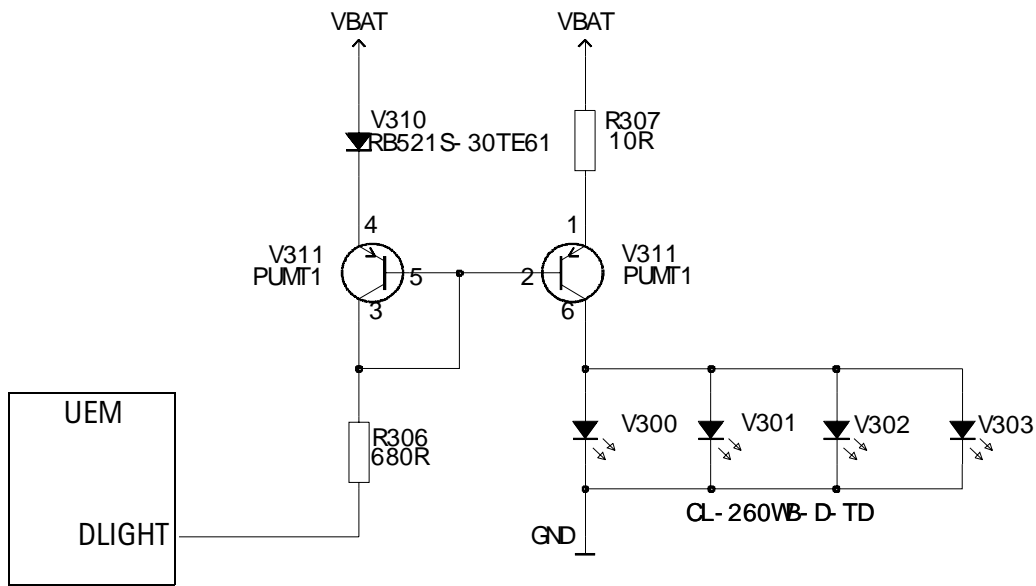


Figure 13 LED driver circuit for display.

Vibra

A vibra-alerting device is used to generate a vibration signal for an incoming call. The vibra is placed in the top of the phone. It is fastened to the A-cover by means of two wings that are pressed into the A-cover.

The vibra is electrically connected to the PWB by spring contacts.

The vibra is controlled from the UEM by a PWM (Pulse Wide Modulated) square wave signal.

Buzzer

Alerting tones and/or melodies are generated by a buzzer, which is controlled by a PWM signal from the UEM.

The buzzer is designed to a first resonant peak at 2500 Hz. The ringer melodies will be optimised in MCU so the main frequency of any given melody is shifted to near the resonant peak. For this optimisation a program called BuzzCalc will be used for the calculation of the dominating frequency of a given ringing melody or tone.

The design of the buzzer is a direct copy from the NPE-3 project. The Buzzer is glued to a gasket. Vendor delivers this final assembly. Sound holes are placed in the A-cover

The buzzer is electrically connected to the PWB by spring contacts.

Keypad

See keypad interface in section Keypad interface on page Keypad interface.

IR-module

The IR module CIM-93M4 is fully compliant with the IrDA1.2.a and supports data rates of 9600 bps to 1152 kbps. The module is connected to the UEM IR module, which acts as a level-shifter between the IR module and the UPP. The UEM IR module supports the data rates of the CIM-93M4.

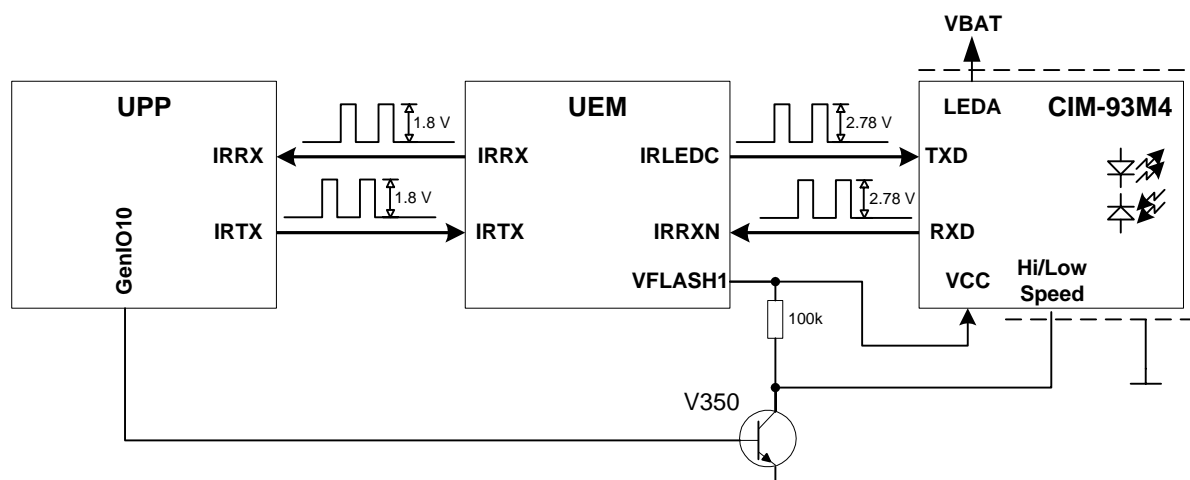


Figure 14 NPL-1 IR connectivity

CIM-93M4 operates on 2.7 V logic, thus the transistors.

SIM

NPL-1 uses a product specific SIM-card reader (SIM reader). Electrical connection of SIM reader is similar to other DCT4 products. The SIM interface is split between UEM and UPP (see Figure 7.14 UPP, UEM and SIM Connections below). This has been done in order to reduce the amount of interconnections on the SIM interface between the UPP and the UEM. The SIM interface control logic and UART is integrated into the UPP. The SIM interface start-up and power down sequence, including timing and reset generation is implemented in UEM. The SIM interface in the UPP supports the SIM speed enhancement features, which improves the data transfer rate in the SIM interface.

The UEM contains the SIM interface logic level shifting. UPP SIM interface logic levels are 1.8V. The SIM interface can be programmed to support 3V and 1.8V SIMs. A 5V SIM interface is *not* supported. A register in the UEM selects the SIM supply voltage. It is only allowed to change the SIM supply voltage when the SIM IF is powered down.

The SIM power up/down sequence is generated in the UEM. The Battery Type contact signal (BSI) is used to recognise if the battery suddenly is removed from the transceiver

block. The SIMCardDet is not used. If the BSI goes low, the power down sequence is automatic initiated. The SIMIF will then force all the connections low, i.e. SIMRST, SIMCLK, SIMDATA and VSIM. A comparator inside the UEM does the monitoring of the BSI signal. The comparator offset is such that the comparator output does not alter state as long as the battery is connected. The BSI comparator threshold level is 2.1 V with 75 mV hysteresis.

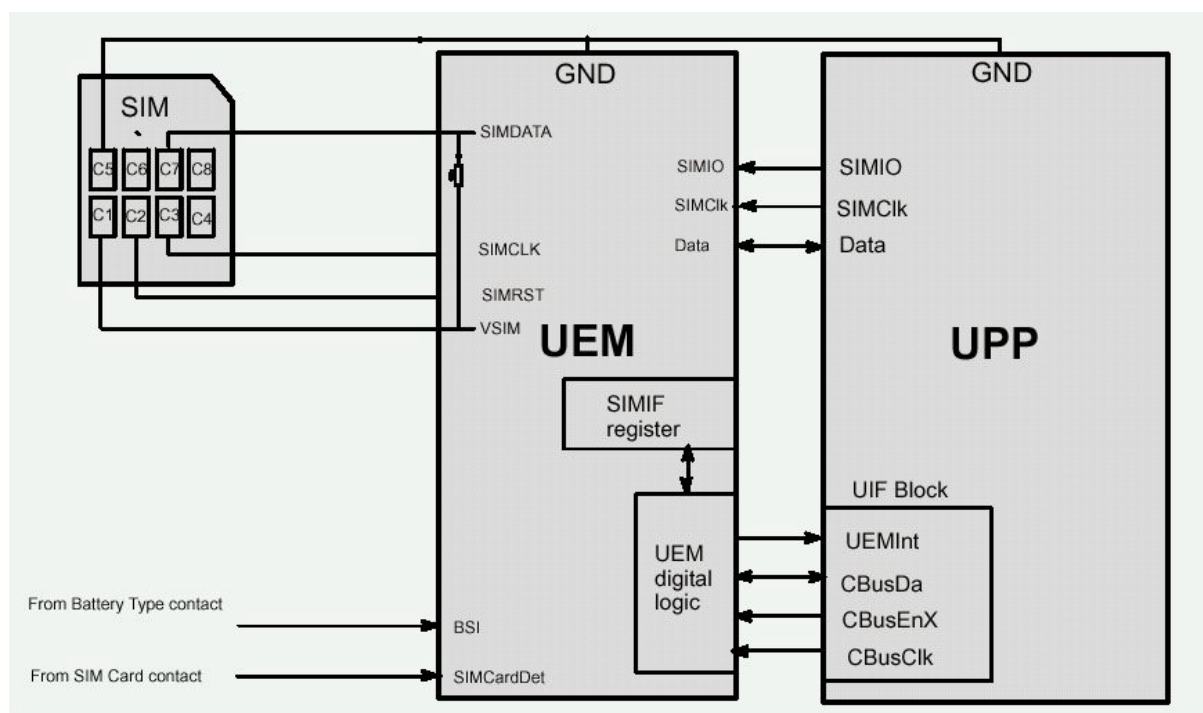


Figure 15 UPP, UEM and SIM Connections

Memory description

The NPL-1 baseband consists of 64Mbit (8MB) external flash memory. Access to the flash is performed as 16-bit access in order to improve the data rate on the bus.

The purpose of the memory interface is to reduce the amount of connections by multiplexing the address and data bus on to the same signals. If the memory address space is more than 16 bits, which is the case, then 16-bit data can be multiplexed on the address inputs. This requires the memory to store the address during the first cycle in the access as described in Figure 8.1 Basic reading (Random access).

In addition to this, the system provides a Power Save signal (PS), which is used to reduce the switching on the external bus between the memory and the UPP. In case of writing to the flash, the UPP provides the information on the PS signal, and in case data is read from the flash, the memory provides the status of the PS signal. The PS signal is used to indicate if data should be inverted at the receiver end. If PS = "1" the data shall be inverted at the receiver end before it is stored/processed. The PS-signal will be described more in details in section Power saving signal (PS)..

Furthermore the memory is capable of handle burst-mode (multiplexed address/data-bus) and memory blocking, which is controlled by the UPP.

Read cycle.

The read cycle is initiated by first applying the address to the multiplexed address/data-bus. The address is latched at the rising edge of the AVD-signal. The memory device captures the address/data bus-state at point B. The captured data is compared on a bit by bit base (MSB–MSB, LSB–LSB), with the data inside memory. If the comparison shows more equal bits than unequal bits, the data is not inverted before it is send out on the address/data bus as output data. The result of the comparison is indicated, by using the PS signal before the data is read (at point C) by the Bus Controller. This allows the receiving device to invert the data before it is read into a register. The valid PS signal needs to be available in advance before the actual read operation takes place.

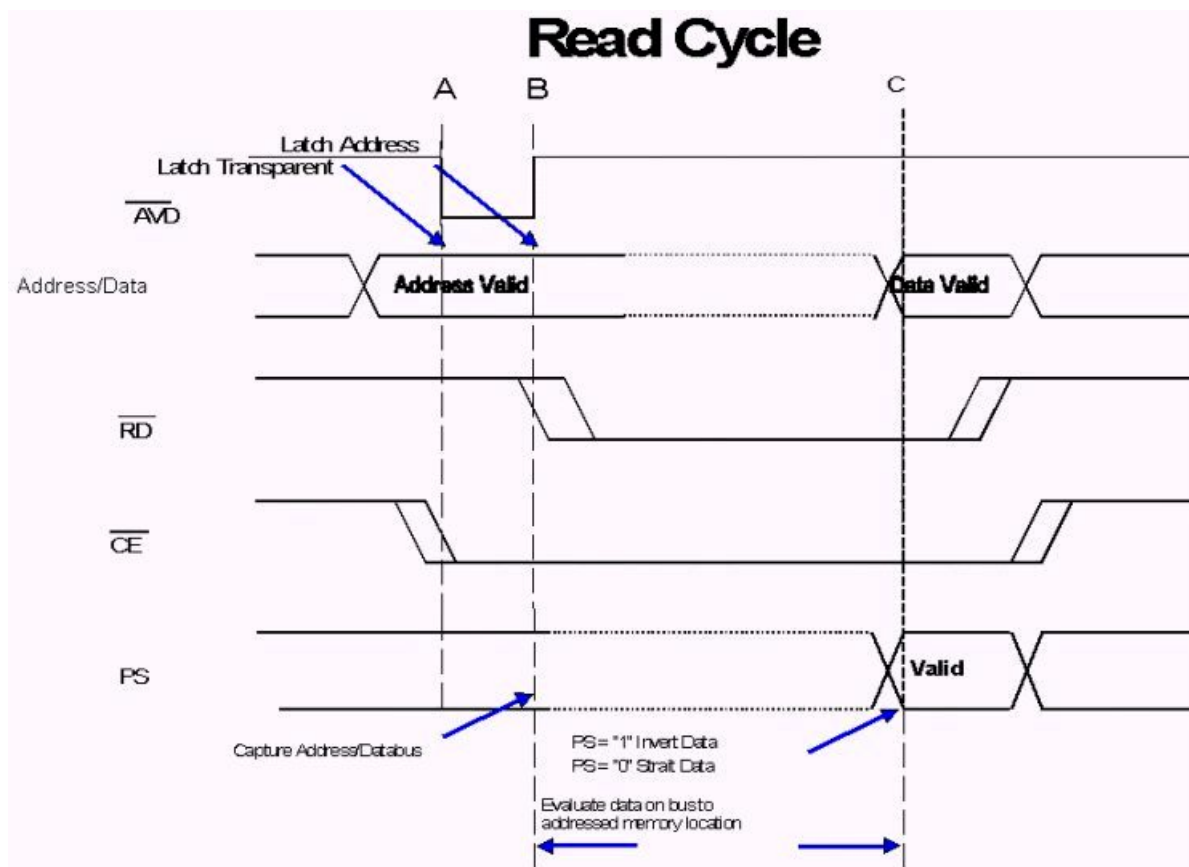


Figure 16 Basic reading (Random access)

Write cycle.

The write cycle is initiated by first applying the address to the multiplexed address/data bus and to the address lines Axx-A16, (Axx is the MSB address for that memory density). The address latch is transparent from A to B. The address is latched at the rising edge of the AVD signal. Latching address Axx-A16 is mandatory. The random access time is measured from a stable address, falling-edge of AVD or falling-edge of CE which ever occurs last. No clock is provided for a random access.

The below figure shows a basic write waveform.

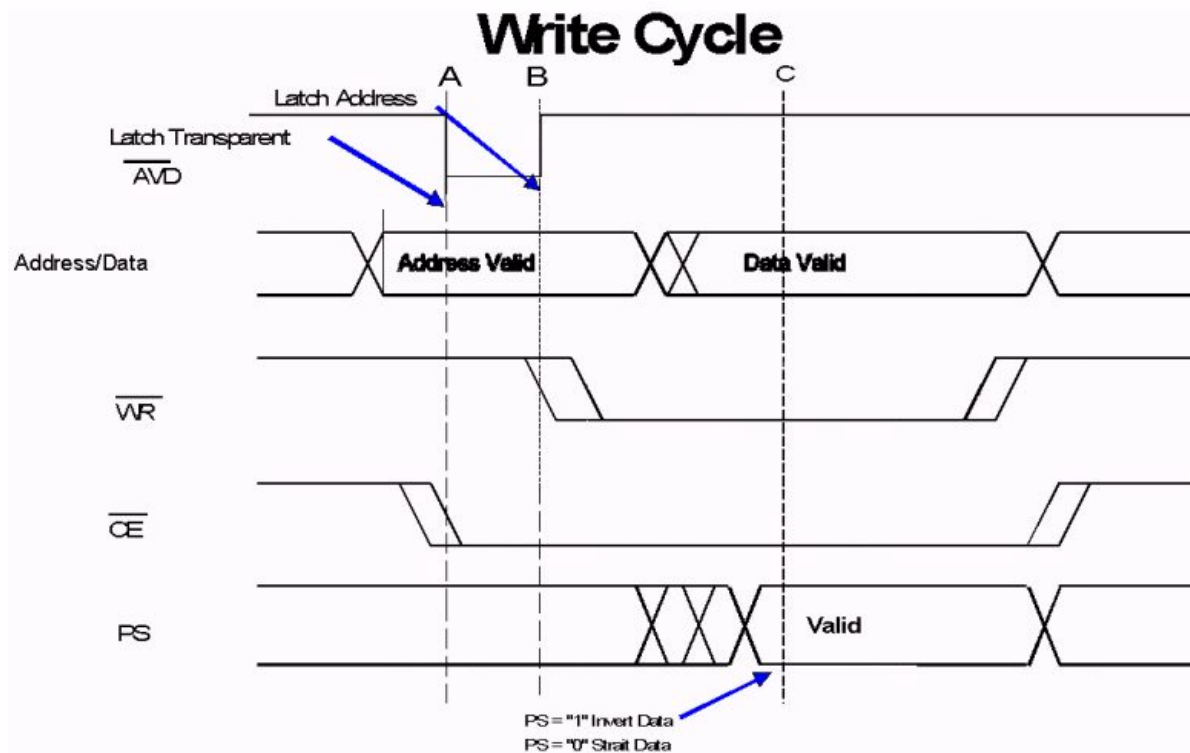


Figure 17 Write waveform (Random access)

Power saving signal (PS).

In order to reduce the power consumption on the bus a Power Save function is introduced. This function reduces the amount of switching on the external bus.

Power is consumed in a digital system when a signal changes state. The power is consumed when the capacitive load is either charged or discharged. The capacitive load is introduced by the interconnection itself and of cause by the input at the receiving device. Internally in digital circuits the capacitive load is lower, than at the interconnect level at the printed circuit board. Therefore it is an advantage if the amount of changes on the external interconnection, i.e. between two digital circuits, can be minimised. Therefore on a wide bus like an address/data bus in a microprocessor system, power is saved, if the data to be transmitted on the external bus, causes a minimum amount of transitions. This can be achieved by comparing the previously data on the bus, with the data to be transmitted, and *if* inverting the data to be transmitted causes less transitions to be performed on the external bus, the data is inverted, before it is output on the data bus. To inform that the data is inverted, a control signal is used to inform the receiving device, that the data must be inverted before any further processing.

Data on the address/data bus is bit wise compared which means that the data previously on DO (DOe) is compared with the new data to be output on DO (DOi). If the two data elements are the same (DOe=DOi) a logic "0" is indicated to the comparing device. If the two data elements are not the same (DOe=NOT(DOi)) a logic "1" is indicated to the comparing

device. If there are more equal signal than unequal signals on the address/data bus, the new data is not inverted before it is sent out on the bus. If there are more unequal than equal data on the address/data bus, the data is inverted before it is sent out on the bus. The status whether the data that is presented on the address/data bus is inverted or not, is indicated by a separate signal to the memory device. If the data on the bus is not inverted this power control signal (PS), is at logic "0" state. If the data that is presented on the bus is inverted, this is indicated by PS = logic "1". This PS signal is a common signal for all the devices connected to the address/memory bus. The transmitting device uses the PS signal to indicate non-inverted or inverted data. As only one device at a time, can present data on the address/data bus, this signal is shared and only one additional control signal PS is needed for the address/data bus, although the data bus may be connected to several devices. The below figure shows how this PS-signal actually works.

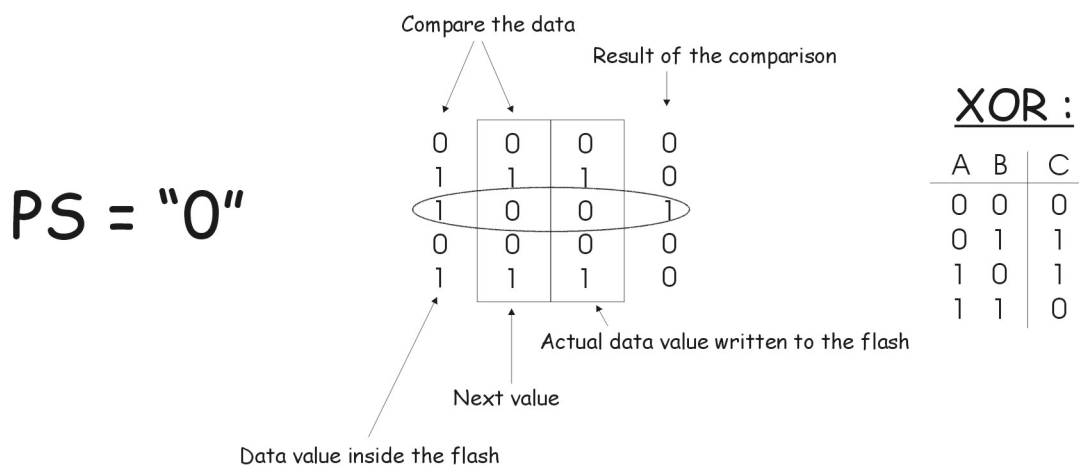


Figure 18 The data is compared by using an XOR-function. The result can be seen above.

In Figure 18 there are more equal bits than unequal bits, so therefor the data is not inverted before it is sent out to the flash. This means that the PS-signal is "0". The next scenario shows the opposite situation.

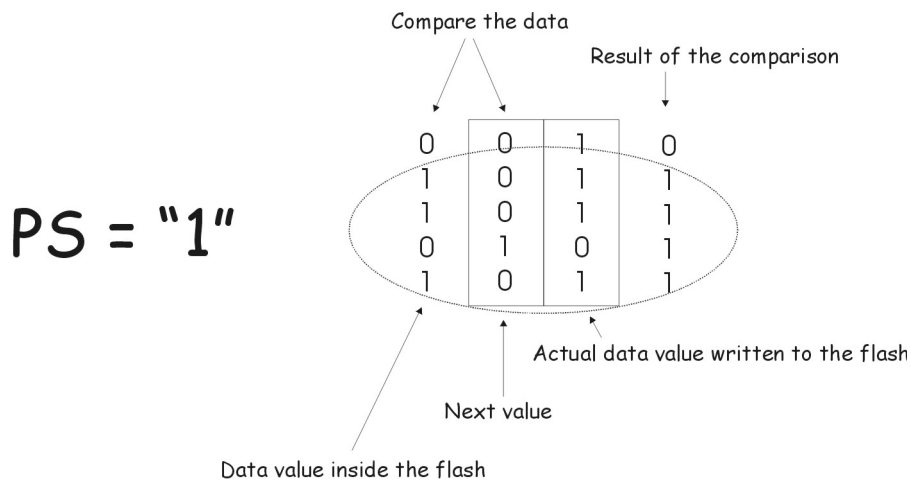


Figure 19 The comparison shows more unequal bits than equal bits, and the bits are inverted on the bus.

The power save (PS) function is only active in burst mode due to delay in the readings (Random access). If it were used in random access, it would have introduced a delay of 10 – 15 ns. The PS is not activated in the first access in the burst, only from the second access in the burst.

In particular in burst mode it is important to keep the performance. In order to reduce complexity in the memory, the power save function does not apply to the address. This means that the address will always be presented in its true value. This means that the memory do not have to manage the inversion of the address. In case of burst access it is possible to reduce the power on the external bus by comparing the contents of the data in the burst, not with the data on the bus. This results in that the random access data is presented on the bus, as such but the following data in the burst is presented using the power save function. By pipelining the power save information in this manner the additional delay caused by the comparison logic is removed.

Memory block.

The memory or flash is organised in four Banks, A, B, C and D. Bank A and B each contain eight 8 Kword sectors and thirty-one 32 Kword sectors. Bank C and D each contain thirty-two 32 Kword sectors. The total sector Architecture is eight 8 Kword sectors and one hundred twenty-six 32 Kword sectors.

Block locking.

To prevent accidental writings to some of the sectors in the flash, block locking has to be used. This can, depending on the vendor, be implemented by using different methods. AMD and Intel are the to only vendors that NPL-1 is going to use for the flash purpose. AMD and Intel will implement their block locking in the following way.

Intel: The locking scheme offers two levels of protection. The first allows software-only control of block locking (useful for frequently changed data blocks) while the second requires hardware interaction before locking can be changed (protects infrequently changed code blocks). For this purpose, a dedicated pin called WP is used. The WP-pin or signal is only controlled by the hardware.

Lock block:

The blocks' default power-up or reset status is locked. Locked blocks are fully protected from alteration. Attempted program or erase operations to a locked block will return an error in a status register inside the flash. A locked block's status can be changed to unlocked or lock-down using the appropriate software commands. Writing the "Lock block command" sequence can lock an unlocked block.

Unlock block:

Unlocked blocks can be programmed or erased. All unlocked blocks return to the locked state when the phone is or powered down. An unlocked block's status can be changed to the locked or locked-down state using the appropriate software commands. A locked block can be unlocked by writing a "unlock block command" sequence, if the block is not locked-down.

Lock-down block.

Locked-down blocks are protected from program and erase operations (just like locked blocks), but software commands alone cannot change their protection status. A locked-down block can only be unlocked when the WP-signal is high. When the WP-signal goes low, all locked-down blocks revert to locked. A locked or unlocked block can be locked-down by writing a "Lock-Down Block command" sequence. Locked-down blocks revert to the locked state at device reset or power-down.

AMD: All blocks have a locking latch and upon power up all blocks are locked. To unlock a block a command sequence must be written, once the command unlock sequence is written the SW can unlock as many blocks as required by entering the block address while keeping a specific address high. If the address is taken to low, the block will be locked instead of unlocked. The SW locking is similar to the Intel SW locking.

The AMD flash does also have the same hardware lock as Intel. The signal or pin is called WP (write protect). The blocks are locked if WP is set to low. If the WP-signal is set high then the SW can control the locking of the blocks. Finally, if the VPP pin is set to low all blocks are locked.

It is not yet specified which flash type NPL-1 is going to use, but the SW-team has to implement one of the above block-locking methods.

Read while Write (RWW).

The device is capable of reading data from one Bank of the memory while programming or erasing in the other Bank of the memory. An erase operation may also be suspend to read from or program to another location within the same Bank (except the sector being erased).

Burst mode.

The flash device supports burst-mode. The purpose is to improve the data rate between the flash and the UPP. The burst-mode can only be used for read operations. It is possible to access the memory in burst-mode over the entire memory except for the 8 x 8 Kbytes sectors. When using burst-mode at least 4 word (4*16 bits) is read from the flash. A read operation from the flash, normally first set-up the address, and then the UPP will get the data from this particular address. The address has to be set-up or sent to the flash every time the UPP wants to read from the flash. By using burst-mode the address only needs to be sent one time, then flash will keep sending data as long as there is a clock-signal.

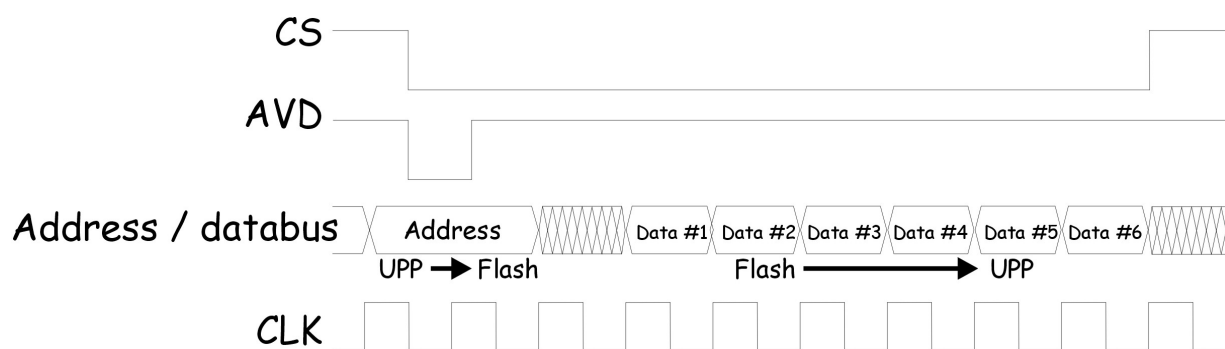


Figure 20 Burst-mode reading from the flash. Note that the address only is sent ones. The flash keeps sending data to the UPP as long as the CS-signal and CLK are valid.

Flash programming.

The actual programming is indicated to the UPP by using the MBUS_RX signal between the UPP and the UEM. The MBUS signal from the UEM to the flash prommer (FPS8 box) is used as clock for the synchronous communication. The flash prommer keeps the MBUS line low during UPP boot, to indicate that the flash prommer is connected. If the UPP MBUS_RX signal is low on UPP, the MCU enters flash programming mode. If the signal is high, the MCU starts loading software from the flash.

In order to avoid accidental entry to the "flash programming mode" the MCU only waits for a specified time, to get input data from the flash prommer. If the timer expires without any data being received, the MCU will continue the boot sequence. The MBUS signal from UEM to the external connection is used as clock during flash programming. This means that flash programming clock is supplied to the UPP on the MBUS_RX signal. The flash prommer indicates to the UEM that flash programming/reprogramming by writing an 8 bit password to the UEM. The data is transmitted on the FBUS_RX line and the UEM clocks the data on the FBUS_RX line into a shift register. When the 8-bits have been shifted in the register, the FPS8-box generates a falling-edge on the BSI line. This loads the shift register content in the UEM into a compare register. These 8-bits will be compared in a register to see if they match the "secret" default value inside the UEM. At this point the flash prommer must pull the MBUS signal to UEM low, in order to indicate to the MCU that the flash prommer is connected. The UEM reset-state machine performs a reset to the system (PURX low for 10–100 ms). The UEM "flash programming mode" is valid until MCU sets a bit in the UEM register, which indicates the "end of flash programming". Setting this bit also clears the compare register in the UEM previously loaded, at the falling edge of the BSI signal. During the "flash programming mode" the UEM watchdog is disabled. When the bit is set it indicates "end of flash programming" and it resets the UEM watchdog timer to it's default value. Clearing the flash programming bit also causes the UEM to generate a reset to the UPP. The BSI signal is used to load the value into the compare register. In order to avoid spurious loading of the register, the BSI signal will be gated during UEM "master-reset", and during "power-on" when PURX is active. The BSI signal should not change state during normal operation unless the battery is extracted, in this case the BSI signal will be pulled high, note a falling edge is required to load the compare register.

MCU Boot.

When the MCU boots, it looks for flash programming indication by reading the status on the MBUS signal. If this signal is pulled low the MCU sets up the UART in synchronous mode, and indicates to the flash prommer, by setting FBUS_TX low, that it is ready to accept the secondary boot-code. All flash programming related SW that is downloaded is done so to the UPP internal MCU SRAM. The MCU also ends up in "flash programming mode", if the contents of the flash is empty (reading FFH from the first memory location in the flash).

Flash Identifiers.

Due to that DCT4 supports many different manufacturers; NMP needs to have so called flash identifiers. The flash identifier tells the MCU which HW environment it is working in, and also block size and configuration of the flash.

First Word.

The word contains the information about the number of flash devices connected to the UPP. It is possible to setup the UPP so that it supports two devices. The MSB bit in the word indicates the amount of flash devices used by the baseband. The amount of wait states for the random access is specified over 3-bits in this word. The amount of wait states is specified related to the system clock used in that system. The MCU PLL factor is also specified in this word (2-bits).

Second Word.

This word contains information about flash sectors available for EEPROM emulation. If no RWW capability is indicated, this field then contains information of the serial EEPROM that is used in the system.

Third Word.

This word contains similar information as the first word but for the second flash if such is used.

Fourth Word.

This word contains information about the sector configuration of the second flash.

Fifth Word.

This word contains information of the external SRAM if it is available on the baseband, the size of it and the amount of wait states to be used when accessing it.

Absolute maximum ratings (AMD 64Mbit).

Table 7: Absolute maximum ratings for AMD 64 Mbit

Parameter	Rating	Remarks
Supply voltage (V_{cc}) (operational voltage is: 1.7 –1.9)	-0,5 V to +4,0 Volt	Minimum DC voltage on input or I/O pins is -0.5 V
VPP and RESET	-0.5 V to +12.5 Volt	Minimum DC input voltage on pins VPP, and RESET is -0.5 V
Output Short Circuit Current	100 mA	No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.
Voltage with Respect to Ground. All pins except VPP and RESET	0.5 V to $V_{cc} + 0.5$ Volt	Minimum DC voltage on input or I/O pins is -0.5 V

Absolute maximum ratings (INTEL 64Mbit).

Table 8: Absolute maximum ratings for INTEL 64 Mbit

Parameter	Rating	Remarks
Voltage on any pin (except Vpp, Vpp)	-0.5V to +2.45V	See reference for details
Vpp Voltage	-0.2V to +14V	
Vcc and Vccq	-0.2V to +2.45V	
Output short circuit current	100mA	

HW Interfaces

Keypad interface

The NPL-1 phone doesn't have separate keyboard PWB. The keys are directly connected via the KEYB(10:0) bus to the UPP. The keypad consist of a 5x4 matrix, meaning 5 rows (R0 – R4) and 4 columns (S1 – S4).

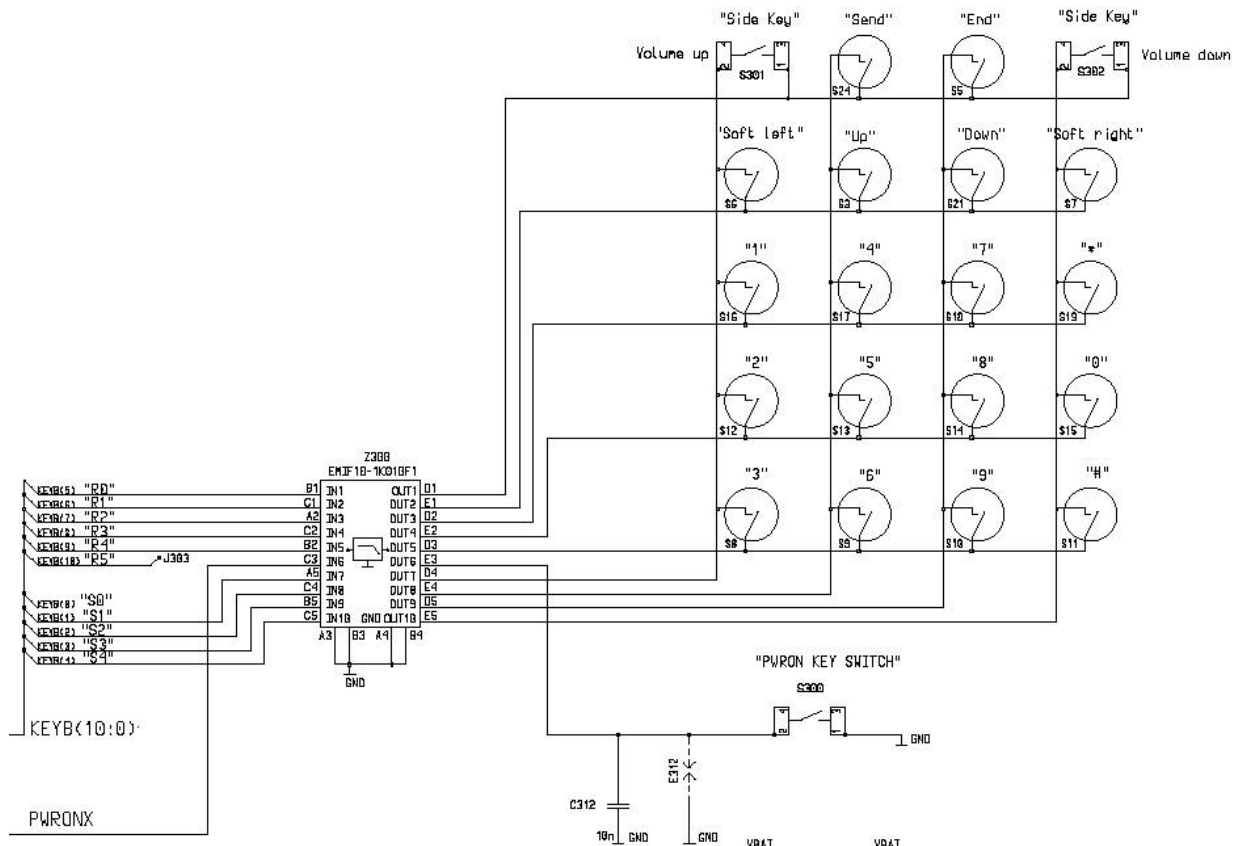


Figure 21 NPL-1 keypad

When there is no key pressed, all the inputs from the rows are high due to that the UPP has internally pull-up resistors on those lines. All the columns are low at this state. When a key is pressed, the specific row where the key is placed is pulled low. This generates an interrupt to the MCU and the MCU now starts its scanning procedure. The procedure first set all the columns high (KEYB (0) to KEYB (4)) and then one by one set them low again. Only one of the columns is low at the time. While one of the columns is low, the row is (KEYB (5) to KEYB (10)) is read by MCU to find the active low signal. If the input is low the MCU knows that a key is pressed. When the key has been detected all the keypad-register inside the UPP is reset and it's ready receiving new interrupt.

LCD Interface

LCD connection from main PWB to FPC contact on LCD is made with an 8-pin spring connector (same as in Hda12).

Table 9: LCD Module pin-out to PWB

Pin	Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
1	XRES	t_{rw}	Reset			$0.3 \times V_{DDI}$	V	Logic Low, active
				1000			ns	for valid reset
2	XCS	t_{CSS} t_{CSH}	Chip Select	$0.7 \times V_{DDI}$			V	Logic High
						$0.3 \times V_{DDI}$	V	Logic Low, active
				60			ns	setup time
				100			ns	hold time
3	VSS	GND	Ground		0		V	
4	SDA	t_{sds} t_{sdh}	Bi-directional serial interface	$0.7 \times V_{DDI}$			V	Logic High
						$0.3 \times V_{DDI}$	V	Logic Low
				100			ns	Data setup time
				100			ns	Data hold time
5	SCLK	t_{scyc} t_{shw} t_{slw}	Serial clock input	$0.7 \times V_{DDI}$			V	Logic High
						$0.3 \times V_{DDI}$	V	Logic Low
				250			ns	Serial clock cycle (4MHz)
				100			ns	Serial clock high pulse width
				100			ns	Serial clock low pulse width
6	VDDI		VDD digital power supply	1.6	1.8	1.88	V	
7	VDD		Booster power supply	2.6	2.78	2.86	V	
8	VOOUT		Booster output			12	V	Decoupled to Vflash1 on main PWB with 1uF

SIM interface

The SIM interface supports both 1.8V & 3V with 255 entries. The figure below shows the placement of the individual SIM pins.

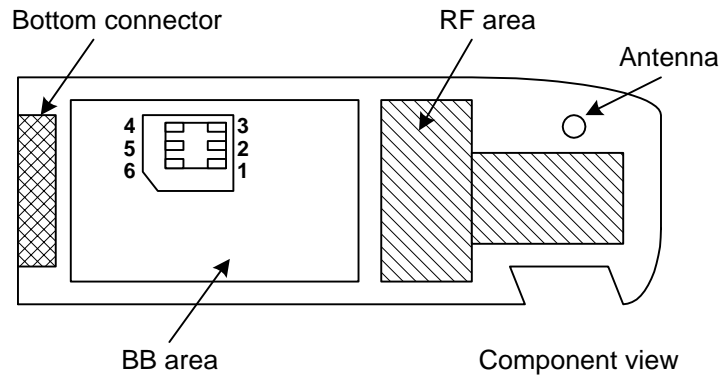


Figure 22 Placement of SIM pins (Phone bottom view)

Table 10: SIM Connector Interface

Pin	Name	Parameter	Min	Typ	Max	Unit	Notes
1	SIMCLK	Frequency T_{rise}/T_{fall}	1.05	3.25	3.36 26	MHz ns	SIM clock
2	SIMRST	V_{oh} V_{ol}	$0.9 \cdot VSIM$ 0		$VSIM$ $0.15 \cdot VSIM$	V	SIM reset
3	VSIM	3V SIM Card	2.8	3.0	3.2 25	V mA	Supply voltage I_{cc} , 4MHz
		1.8V SIM Card	1.6	1.8	2.0 25	V mA	Supply voltage I_{cc} , 4MHz
4	GND	GND	0		0	V	Ground
6	DATA	V_{oh} V_{ol} V_{ih} V_{il}	$0.9 \cdot VSIM$ 0 $0.7 \cdot VSIM$ 0		$VSIM$ $0.15 \cdot VSIM$ $VSIM$ $0.15 \cdot VSIM$	V	SIM data T_{rise}/T_{fall} max 1us

Ostrich

The STI-block, placed in the UPP "brain block", has a trace interface that can be used for tracing messages written by the DSP or the MCU. Writings or reading to a specific I/O register or an address match on the MCU address bus can be traced on the interface. The interface consists of three lines plus a GND line. One of the great advantages, compared to JTAG, is that the SW in the phone can run normally while trace messages is lead out to the Ostrich box. Data can be captured at 40MHz on the interface.

The main purpose for the interface is debugging in R&D phases. It can also be used for flashing interface.

Table 11: Ostrich interface

Signal	Pin (test point)	Min.	Max.	Unit	Remarks
STITxD	J471	0	1.8	Volt	Data to transmit
STISCIK	J472	0	1.8		Clock
STIRxD	J473	0	1.8		Data to receive
VBAT	J470	2.9	5.3		Supply to Ostrich
GND	J474	0			GND

JTAG interface

The JTAG interface is used to monitor and or debug DSP activity. The connections from the UPP are routed to PWB pads, which are free for access.

Table 12: JTAG interface levels

Signal	Pin (test point)	Parameter	Min	Typ	Max	Unit	Remarks
JTMS	J480	Logic "1" Logic "0"	1,2 0		1,8 0,5	Volt	
JRst	J481	Logic "1" Logic "0"	1,2 0		1,8 0,5		JTAG reset.
JTDI	J482	Logic "1" Logic "0"	1,2 0		1,8 0,5		
VIO	J483		1,72	1,8	1,88		JTAG supply voltage
JTDO	J484	Logic "1" Logic "0"	1,2 0		1,8 0,5		JTAG data output
JTCK_ret	J485	Logic "1" Logic "0"	1,2 0		1,8 0,5		JTAG return clock
JTCLK	J486	Logic "1" Logic "0"	1,2		1,8		JTAG clock
EMU0	J487	Logic "1" Logic "0"	1,2 0		1,8 0,5		Emulation pin 0
EMU1	J488	Logic "1" Logic "0"	1,2 0		1,8 0,5		Emulation pin 1
GND	J489			0		JTAG GND	

BT module interface

SW interface

The BT102 component differs from all other components by having its own controlling software. *Bluetooth MCM* represents the controlling SW physically programmed into the BT102 module.

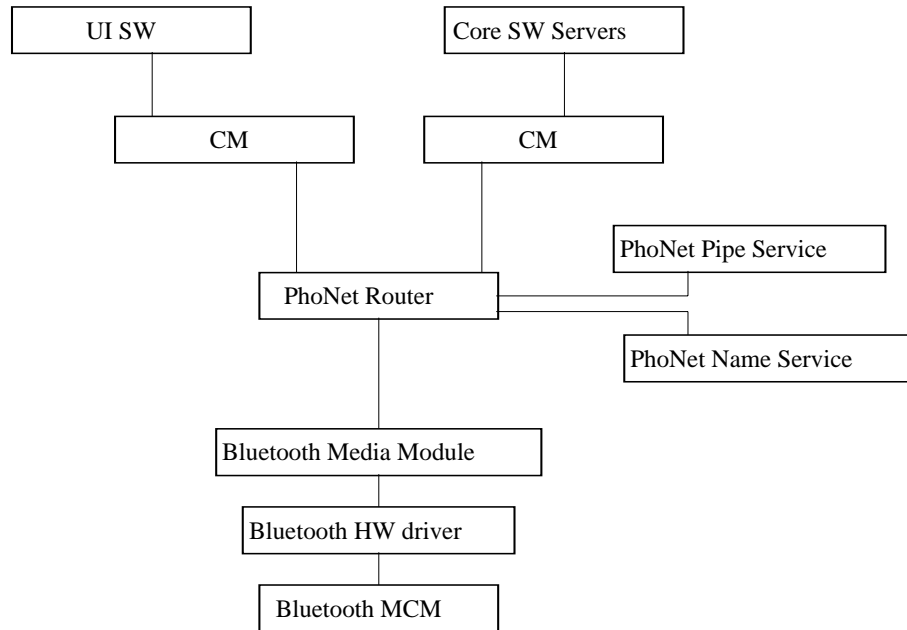


Figure 23 SW interface diagram

BT102 Flash programming

The *Bluetooth MCM* SW needs to be programmed when the module is assembled into the phone. This is implemented by interleaving so that code data is being transferred to the BT102 while the main flash is performing the internal programming of the phone SW.

The figure below illustrates the set-up used for BT102 flash programming.

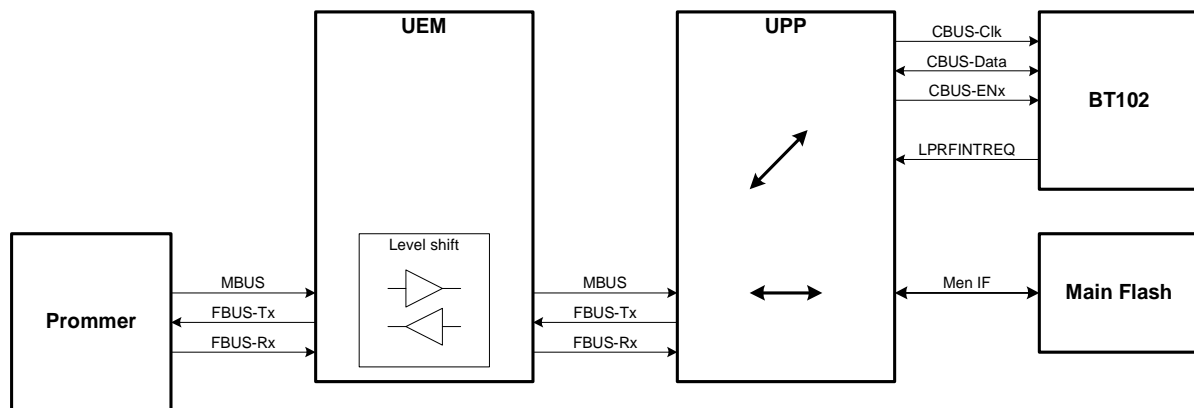


Figure 24 BT102 flash programming

HW interface

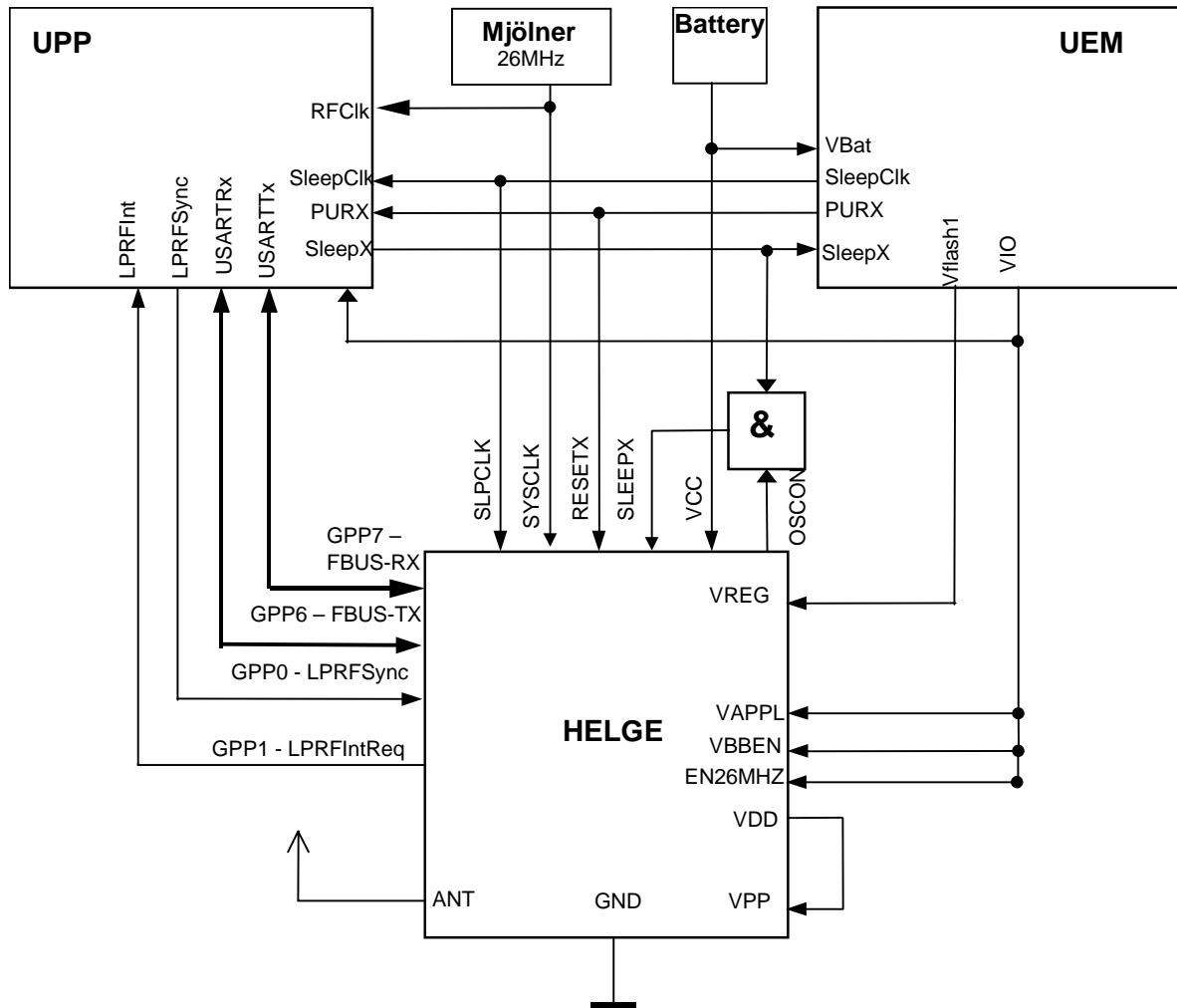


Figure 25 BT102 HW interface

The table below describes the signals covering the interface between the BT module and the engine. The signal names are referring to the NPL-1 schematic diagram.

Table 13: BT – BB interface description

Signal name MCM pin #	From	To	Parameter	Min.	Typ.	Max.	Unit	Notes
RESET								
RESETX 44	UEM PURX	MCM	Logic "1"	1.40		1.80	V	BB reset
			Logic "0"	0		0.20	V	
Clock input								
SYSCLK 50	RF	MCM	Signal amplitude	0.30		0.80	Vpp	System clock input
			Frequency		26		MHz	

Table 13: BT – BB interface description

Signal name MCM pin #	From	To	Parameter	Min.	Typ.	Max.	Unit	Notes
EN26MHZ 18	UEM Vio	MCM	Voltage	1.40		1.80	V	Defines system clock. "1" = 26 MHz
SLPCLK 26	UEM Sleep-Clk	MCM	Logic "1"	1.26		1.80	V	Sleep clock input
			Logic "0"	0		0.54	V	
			Frequency	32763	32768	32773	Hz	
Power control								
VBBEN 49	UEM Vio	MCM	Voltage	1.40		1.80	V	Stan2 regulators enable
SLEEPX 48	AND circuit	MCM	Logic "1"	1.40		1.80	V	Active mode = "1"
			Logic "0"	0		0.20	V	
OSCON 31	MCM	AND circuit	Logic "1"	1.40		1.80	V	Reflects MCM status. Active mode = "1"
			Logic "0"	0		0.20	V	
GND 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 16, 17, 13, 14, 15, 19, 24, 29, 33, 39, 43, 47, 51, 56			Voltage		0		V	Ground reference
VCC 52, 53, 54	Vbatt	MCM	Voltage	2.95		5.20	V	Main power supply input
VREG 6	UEM Vflash1	MCM	Voltage	2.70		2.86	V	Regulated power supply input
VDD 45	MCM	MCM VPP	Voltage		1.80		V	Supply for VPP
VPP 41	MCM VDD	MCM	Voltage		1.80		V	Programming voltage supply
VAPPL 32	UEM Vio	MCM	Voltage		1.80		V	Supply for application IF
RF air								

Table 13: BT – BB interface description

Signal name MCM pin #	From	To	Parameter	Min.	Typ.	Max.	Unit	Notes
ANT 12	MCM	BT ant.	Impedance		50		Ω	Antenna pin
General purpose I/O								
GPP0 38	MCM	LPRFS ync	Logic "1"	1.26		1.80	V	
			Logic "0"	0		0.54	V	
GPP1 37	MCM	LPRFIn t	Logic "1"	1.26		1.80	V	
			Logic "0"	0		0.54	V	
GPP6 28	MCM	USART Rx	Logic "1"	1.26		1.80	V	
			Logic "0"	0		0.54	V	
GPP7 27	MCM	USART Tx	Logic "1"	1.26		1.80	V	
			Logic "0"	0		0.54	V	
GPP10 36	CBUSC lk	MCM	Logic "1"	1.26		1.80	V	
			Logic "0"	0		0.54	V	
GPP11 35	CBUSD a	MCM	Logic "1"	1.26		1.80	V	
			Logic "0"	0		0.54	V	
CENX 34	CBUSE Nx	MCM	Logic "1"	1.26		1.80	V	
			Logic "0"	0		0.54	V	

Baseband – RF interface

The following table describes all the signals in-between the baseband block and the RF block. The signal names can be found on the schematic for the NPL-1 PWB.

Digital Signals

The values indicated in the following table are input requirements of the device in the "to column". In case the output device in the "from column" causes any restrictions it is noted.

Values are referenced to GND unless otherwise specified.

Table 14: Digital signals

Signal name	From	To	Parameter		Min	Typ	Max	Unit	Notes		
RFICNTRL (2:0)			Mjoelner control bus								
RFBUSEN1 RFICNTRL(2)	UPP RFBUSEN1X	Mjoelner RFBUSENX	Logic "1"	Mjoelner input	1.22			V	RF Chip select. Active Low		
				UPP output	1,37		1.88	V			
			Logic "0"	Mjoelner input	0		0.4	V			
				UPP output	0		0,4	V			
RFBUSDA RFICNTRL(1)	UPP RFBUSDA	Mjoelner RFBUSDA	Logic "1"	Mjoelner input	1.22			V	RF serial data. (bi-directional)		
				UPP output	1,37		1.88	V			
				Mjoelner output	1,32			V			
				UPP input	1,32		1,88	V			
			Logic "0"	Mjoelner input	0		0,4	V			
				UPP output	0		0.4	V			
				Mjoelner output	0		0,4	V			
				UPP input	0		0,51	V			
RFCLK RFICNTRL(0)	UPP RFBUSCLK	Mjoelner RFBUSCLK	Logic "1"	Mjoelner input	1.22			V	RF bus clock.		
				UPP output	1,37		1.88	V			
			Logic "0"	Mjoelner input	0		0.4	V			
				UPP output	0		0,4	V			
			Clock Speed				13			MHz	
			GENIO (28:0)			General purpose I/O					
TXP GENIO(5)	UPP GENIO5	Mjoelner TXP	Logic "1"	Mjoelner input	1.22			V	Transmitter power control enable.		
				UPP output	1,37		1.88	V			
			Logic "0"	Mjoelner input	0		0.4	V			
				UPP output	0		0,4	V			
RESET GENIO(6)	UPP GENIO6	Mjoelner RESET	Logic "1"	Mjoelner input	1.22			V	Reset to RF chip. Active low.		
				UPP output	1,37		1.88	V			
			Logic "0"	Mjoelner input	0		0.4	V			
				UPP output	0		0,4	V			

Analogue Signals

The values indicated in the table below are input requirements of the device in the "to

column". Values are referenced to gnd unless otherwise specified.

Table 15: Analogue signals

Signal name	From	To	Parameter	Min	Typ	Max	Unit	Notes
Clock			System clock for LPRF and phone					
LPRFCLK	Lprfclk buffer	BT102 module SysClk	Frequency		26		MHz	System clock for the Bluetooth module.
				-20		+20	ppm	
			Duty cycle	30	50	70	%	
			Signal amplitude (26 MHz)	0.2	1.0	3.0	V _{pp}	
			Settling time			5,0	mS	VR3 on to stable clock @ MCM input
RFCLK	Mjoelner REFOUT	UPP RFCLK	Frequency		26		MHz	System clock
				-20		+20	ppm	
			Duty cycle	40		60	%	Upp input req.
			Signal amplitude	0,3		1,32	Vpp	Biased in UPP
			DC Offset	0,82	0,9	0,98	Vdc	VR3 on to stable clock @ UPP input
			Settling time			5,0	mS	
RFCONV (9:0)			RF / BB analogue signals					
RXIIIP RFCONV(0)	Mjoelner RXIP	UEM RXIINP	Max input Voltage swing	1.35	1.4	1.45	Vpp	Differential complex RX BB signal
RXIINN RFCONV(1)	Mjoelner RXIM	UEM RXIINN	Nominal Voltage swing				V	
RXQINP RFCONV(2)	Mjoelner RXQP	UEM RXQINP	Input DC level	1.3	1.35	1.4	Vdc	
RXQINN RFCONV(3)	Mjoelner RXQM	UEM RXQINN	Signal frequency		67,7		kHz	
TXIOUTP RFCONV(4)	UEM TXIOUTP	Mjoelner TXIP	Max Differential output swing (ref. TxIN)	2.15	2.2	2.25	Vpp	Differential complex TX signal (programable voltage swing)
TXIOUTN RFCONV(5)	UEM TXIOUTN	Mjoelner TXIN	Input diff. Swing (ref. TxIN)		1,0		Vpp	
TXQOUTP RFCONV(6)	UEM TXQOUTP	Mjoelner TXQP	DC level	1.0	1.20	1.25	Vdc	
TXQN RFCONV(7)	UEM TXQOUTN	Mjoelner TXQN	Source impedance			200	Ω	
			Signal frequency		67,7		kHz	
RFAUXCONV(2:0)			RF / BB analogue control signals					

Table 15: Analogue signals

Signal name	From	To	Parameter	Min	Typ	Max	Unit	Notes
TXC RFAUXCONV(0)	UEM AUXOUT	Mjoelner TXC	Output voltage	0 - 0.1		2,4 - 2.55	V	Transmitter power control
			Source impedance			200	Ω	
			Resolution	10			Bits	
			Reference	Auxref (VrefRF01 ?)				
			Power coef. Range.	0,05		0,94	Vtxc/ Vtxc_max	
			Recom. Power Coef. * @ pwr.lvl.5 (0 pcn)	0,7		0,9	Vtxc/ Vtxc_max	
			Recom.Power Coef. @ pwr.lvl.19 (15 pcn)	0,1		0,2	Vtxc/ Vtxc_max	
			Recom.Power Coef @ Base level	0,1		0,2	Vtxc/ Vtxc_max	

* Power coefficient is defined as the relative TXC voltage level wrt. Max voltage. Power coeff.= Actual dac div. By 1023 = actual

Voltage Supplies and References

Table 16: Regulators and references

Signal name	From	To	Parameter	Min	Typ	Max	Unit	Notes
Regulators			RF regulators					
VR1A	UEM VR1A	Mjoelner VDDCP	UEM Output Voltage	4.6	4.75	4.9	V	Supply to : Charge pump
			Mjoelner Input Voltage	2.64	2.78	4.9	V	
			UEM output Load Current	0	*	5	mA	
			UEM Load Capacitance	800	1000	1200 †)	nF	
				20		600	mΩ	ESR
Settling Time				$300 \cdot t_{d2}$		uS	Sleep to Active	

Table 16: Regulators and references

Signal name	From	To	Parameter	Min	Typ	Max	Unit	Notes
VR2	UEM VR2	Mjoelner VDDTX VDDDIG	UEM Output	2.70	2.78	2.86	V	Supply to : TX – chain Modulator RF-BB digital interface
			Mjoelner Input Voltage	2.64	2.78	2.86	V	
			Load Current	0.1	#	100	mA	
			Load Capacitance	800	1000	1200)	nF	
				20		600	mΩ	ESR
Settling Time	10			uS	Sleep to Active			
VR3	UEM VR3	LPRF-CLK driver & Mjoelner VDDXO VDDBBB	UEM Output voltage	2.70	2.78	2.86	V	Supply to : LPRFCLK driver, XO and baseband buffer
			Mjoelner Input Voltage	2.64	2.78	2.86	V	
			Load Current	0.1)	20	mA	
			Load Capacitance	800	1000	1200)	nF	
				20		600	mΩ	ESR
			Settling Time			100	us	Off to on
10 ?				us	Sleep to Active ?			
VR4	UEM VR4	Mjoelner VDDRXBB	UEM Output voltage	2.70	2.78	2.86	V	Supply to : RX
			Mjoelner Input Voltage	2.64	2.78	2.86	V	
			Load Current	0.1)	50	mA	
VR5	UEM VR5	Mjoelner VDDPRE VDDLO VDDPLL	UEM Output voltage	2.70	2.78	2.86	V	Supply to : Prescaler
			Mjoelner Input Voltage	2.64	2.78	2.86	V	
			Load Current	0.1)	50	mA	
			Load Capacitance	800	1000	1200)	nF	
				20		600	mΩ	ESR
Settling Time	10			uS	Sleep to Active			
VR6	UEM VR6	Mjoelner VDDRXF	UEM Output voltage	2.70	2.78	2.86	V	Supply to : RX
			Mjoelner Input Voltage	2.64	2.78	2.86	V	
			Load Current	0.1)	50	mA	
			Load Capacitance	800	1000	1200)	nF	
				20		600	mΩ	ESR
Settling Time	10			uS	Sleep to Active			

Table 16: Regulators and references

Signal name	From	To	Parameter	Min	Typ	Max	Unit	Notes
VR7	UEM	VCO	UEM Output voltage	2.70	2.78	2.86	V	Supply to : VCO
			Mjoelner Input Voltage	2.64	2.78	2.86	V	
			Load Current	0.1)	45	mA	
			Load Capacitance	800	1000	1200)	nF	
			Settling Time	20		600	mΩ	ESR
			10			uS	Sleep to Active	
VIO	UEM VIO	Mjoelner VDDDL	UEM Output voltage	1.72	1.8	1.88	V	Supply to : RF-BB interface level shifter
			Mjoelner Input Voltage	1.71	1.8	1.88	V	
			Load Current	0.1)	5	mA	
			Load Capacitance					
			Settling Time					
<i>References</i>			<i>RF References</i>					
VREF01	UEM VREF01	Mjoelner VBEXT	UEM Output voltage	1.334	1.35	1.366	V	Used inside Mjoelner as 1.35V reference
			Mjoelner Input Voltage	1.325	1.35	1.375	V	
			Load Current)	100	μA	
			Load Capacitance	800	1000	1200)	nF	
			Settling Time				us	Sleep to Active

*) Typical load current depend on actual RF state.

†) Maximum value according to which the regulator specifications are fulfilled.

Note: The total current from VR1 is 10mA. If only one of the regulators (VR1A or VR1B) is ON, then the current output is 10 mA. If they both are switched ON, the current is 5mA each.

MBus

The default data transmission speed of MBus is 9.6 kbit/s. during flash programming, UEM's digital section generates a "Flash mode" signal. This will set-up the MBus line so that it only can be used for input, and the clock signal from the prommer can be connected. When the FPS8 prommer box is connected to the MBus, the transmission speed is increased up to 6.5 Mbit/s. The data speed can be changed by the SW algorithm inside the box, but the maximum speed is 6.5 Mbit/s.

Table 17: MBus interface

Signal	Parameter	Min	Typ	Max	Unit
MBus	V _{IH}	1.95	2.78	3.0	Volt
	V _{IL}	0	0.2	0.83	
	V _{OH}	1.95	2.78	2.83	
	V _{OL}	0	0.2	0.83	

FBUS

FBUS is an asynchronous data bus having separate TX and RX signals. Default bit rate of the bus is 115.2 Kbit/s. FBUS is mainly used for controlling the phone in the production and for interface to PC via DLR-3 or DAU-9P. Secondly, it can be used for flashing purpose after the production phase.

Table 18: FBUS interface

Signal	Parameter	Min	Typ	Max	Unit
FBUS_RX	V _{IH}	1.95	2.78	3.0	Volt
	V _{IL}	0	0.2	0.83	
FBUS_TX	V _{OH}	1.95	2.78	2.83	
	V _{OL}	0	0.2	0.83	

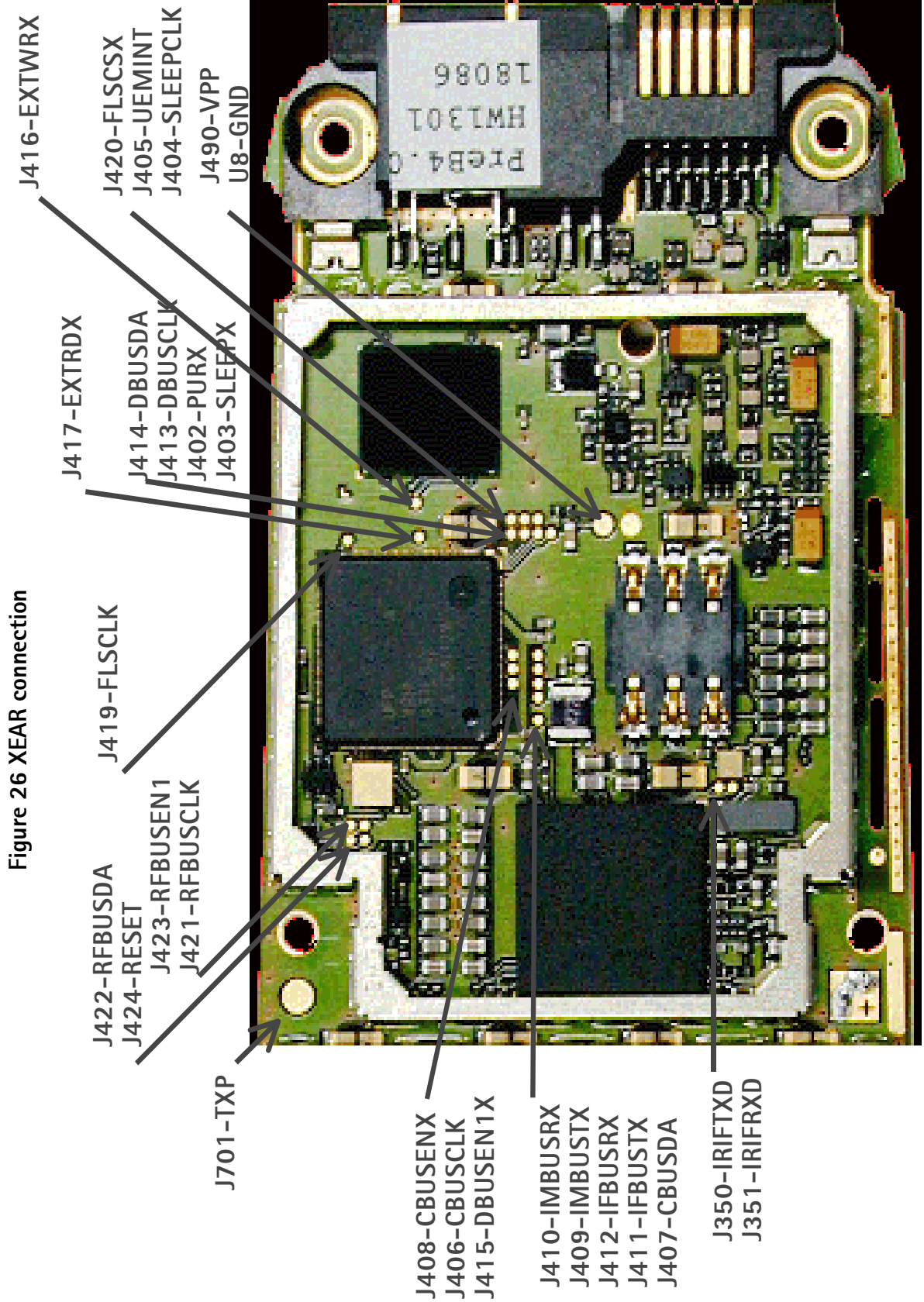
SIM and keypad

For protecting the SIM-card and keypad interface NPL-1 are using special integrated components developed for DCT4 – called ASIP’s. Its an integrated passive array of components which save space and component count. Especially for the SIM reader NPL-1 gain a lot - the capacitance, which normally is a problem on the SIM-clk, is halved compared to NPE-3.

Further details may be found on the NPL-1 schematic diagram.

Test Points

See the following two diagrams for an indication as to where some of the testpoints can be found.



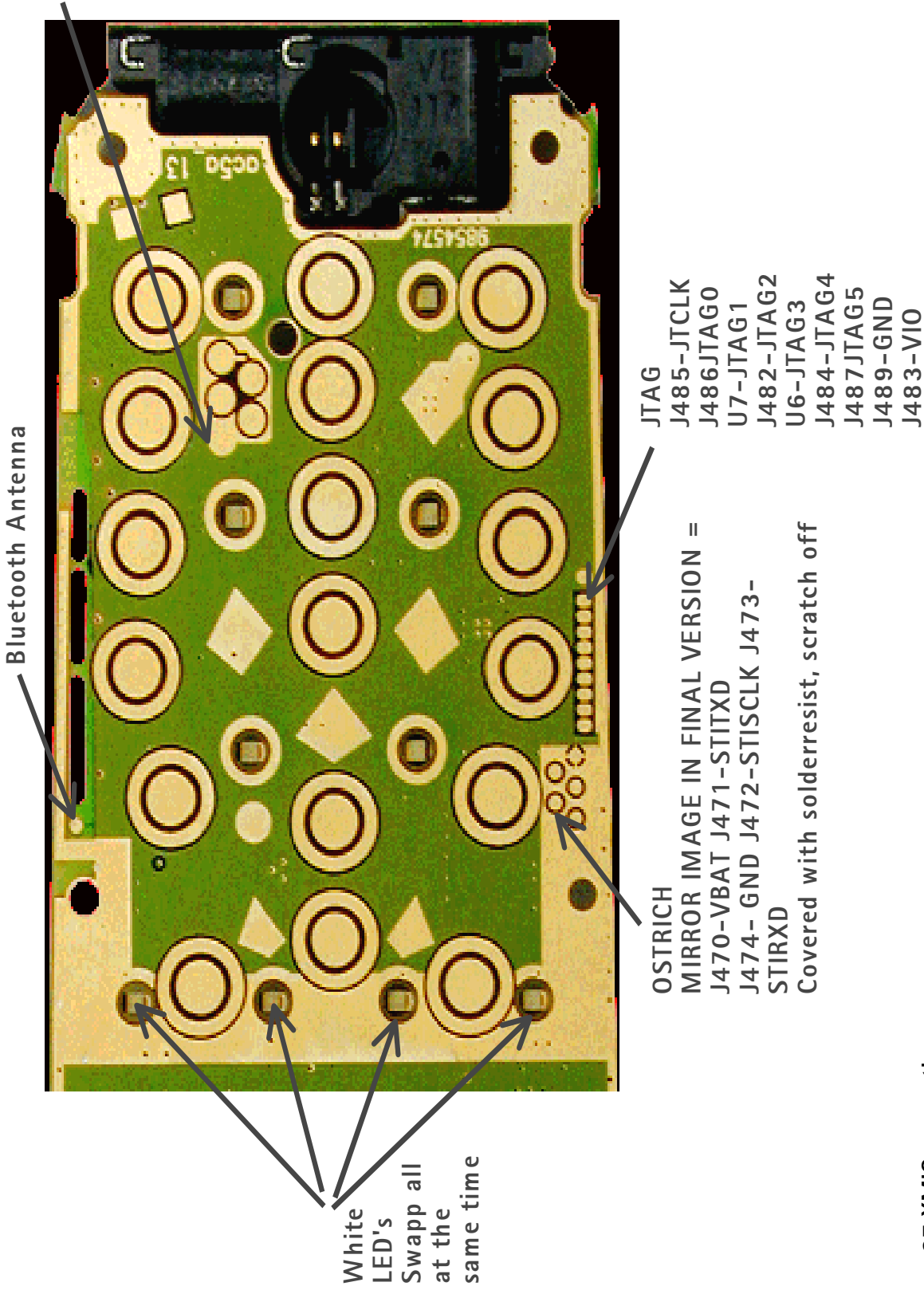


Figure 27 XMIC connection

This page has been intentionally left blank